OPTO ENGINEERING

OPERATION MANUAL

COE-71

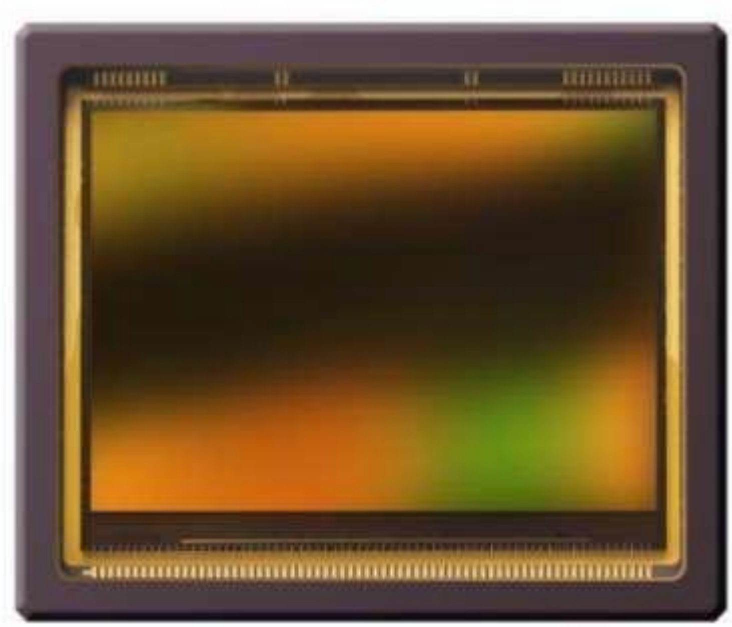
10000 x 7096 Rolling Shutter CMOS

CAMERAS

v 1.3

Rev	Date	Modification
A	2/27/18	COE-71 Original Document

Revisions



COE-71 Precautions

Do not drop, damage, disassemble, immerse, repair or alter the camera.

Applying incorrect power may damage the camera electronics.

The warranty is void if the camera is opened or modified in any way.

Care must be taken in handling as not to create static discharge that may permanently damage the device.

Camera Link is a DC based interface. The camera and capture device must share the same electrical ground. Failure to do so will damage the Camera Link interface chips and/or camera and capture card.

The maximum Camera Link data rate is 85Mhz. This limits the maximum pixel clock speed to 42.5Mhz, which is provided as an overclock mode. Operation is guaranteed at 30Mhz pixel clock and below.

PoCL cables are compatible with the COE-71 camera. PoCL camera power is not supported.

Specifications subject to change without notice.

Contents

Getting Started Camera Link

Camera Power
6-12 V DC Power to the Hirose 6 pin connector.
Mating Connector: Hirose HR10A-7P-6P

PIN	SIGNAL NAME
1	+12V
2	DC Ground
3	Trigger IN
4	STROBE OUT
5	NO CONNECT
6	NO CONNECT

View from Camera Back

Capture Card
Any Base Mode or Medium Mode Camera Link capture card
Such as: BitFlow Axion 1xE.

Imaging SDK
Available from your capture card supplier.

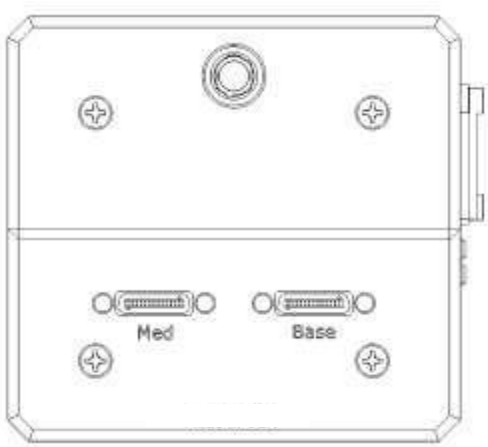
Camera Link Cables
One or two Camera Link cables (Mini HDR to SDR) **must be** rated at 85Mhz or more (two cables for Medium Format).

Camera Communication Software
Opto Engineering Camera Serial Communication Software (GUI)
Download at:
https://www.opto-engineering.com/products/coe-area-scan#Downloads

Getting Started Camera Link

To start imaging with the COE-71 CL:

Install the capture card and software per the capture card manufacturers instructions.
Connect the COE-71 Camera Link cables paying attention to the base and medium connections

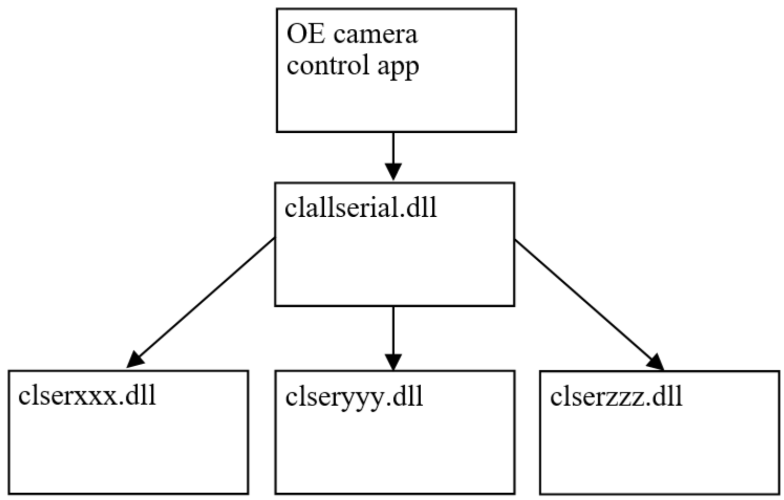


Installing the Opto Engineering Camera Serial Communication Software:

Download and install the Opto Engineering Camera Serial Communication Software (GUI) from https://www.opto-engineering.com/products/coe-area-scan#Downloads

Background:
Per the CameraLink standard, all serial communication is via the .dll clallserial.dll, which dynamically loads the serial communication .dll(s) specific to the frame grabber being used. Opto Engineering installs clallserial .dll in its application directory.

clallserial.dll examines the registry to see where the capture card specific communication dll's have been installed. The naming convention for the capture card specific communication dll's is clser***.dll where *** is the manufacturer specific dll name. The files MUST be in the form clser***.dll in order to be recognized. Some capture card manufacturers will append something like clser***x64.dll for the 64 bit version of the .dll. This file name must be changed to clser***.dll in order to be recognized by clallserial.dll.

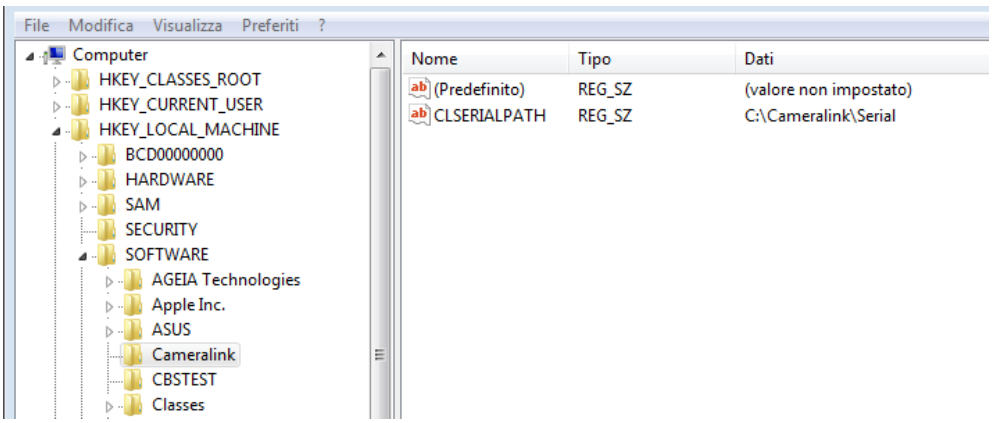


The registry:

When clallserial.dll is loaded by the Opto Engineering serial communication application, it looks at the Registry entry:

HKEY_LOCAL_MACHINE\SOFTWARE\Cameralink CLSERIALPATH.

The location pointed to by CLSERIALPATH is typically C:\Cameralink\Serial, but could be any path that a capture card install might create. It is important to note that the capture card communication dll(s), clser***.dll must be at this path location. clallserial.dll should NOT be in this location.



If the capture card communication dll is spec 1.1 compliant, the user will find this directory already created.

The Opto Engineering control app installs clallserial.dll for the appropriate operating system in the application folder. Depending on the application version, some documentation may be installed in the application folder as well.

If the registry entry above does not exist, create it as well as the directory C:\CameraLink\Serial

In either case, copy-paste the clser***.dll files to C:\CameraLink\Serial

Installing prerequisite software:

The status of these items can be checked in the Control Panel -> Programs and Features listing. If necessary download and install the following prerequisites.

1. **.NET Framework 4.5** to be installed from:

   https://www.microsoft.com/en-us/download/details.aspx?id=30653

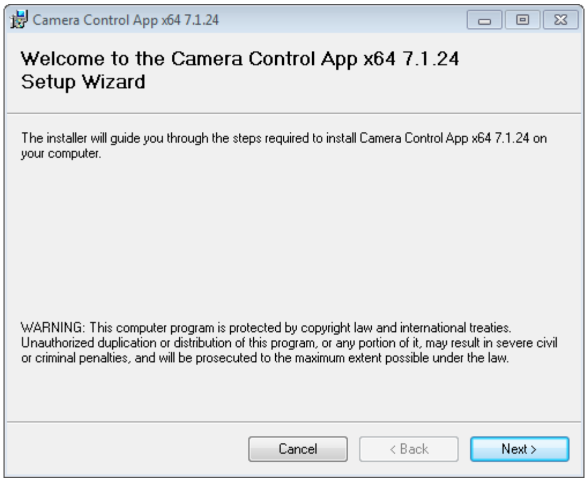
2. **Visual C++ 2010 Redistributable** from:

   https://www.microsoft.com/en-us/download/details.aspx?id=14632

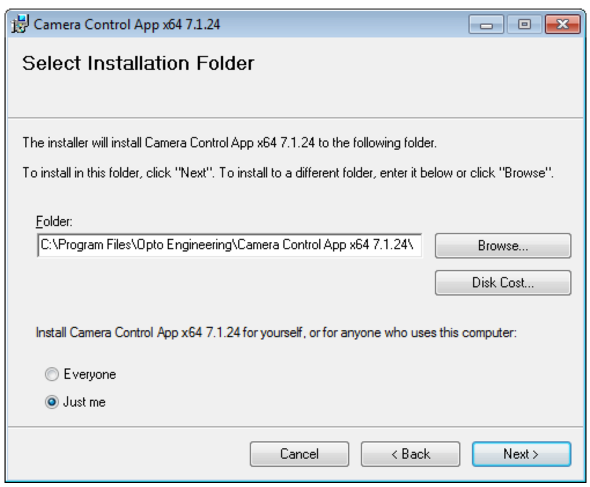
3. **Visual C++ 2013 Redistributable** from:

   https://www.microsoft.com/en-us/download/details.aspx?id=40784

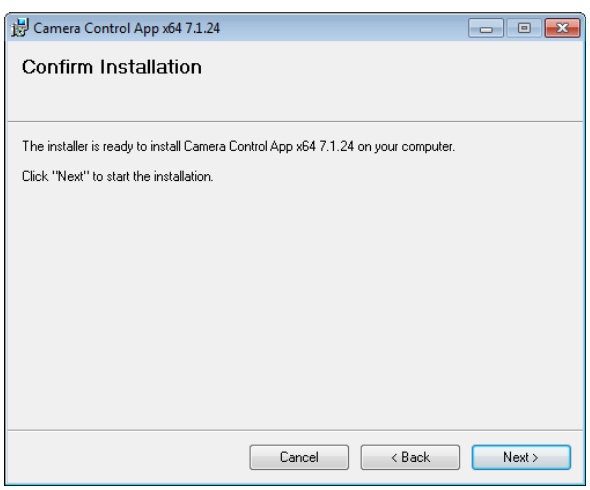
Install the Camera Serial Communication Software:



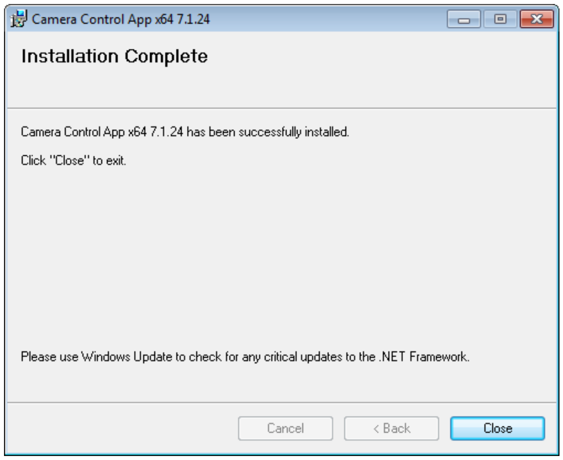
Launch the installer



Select the installation folder



Confirm



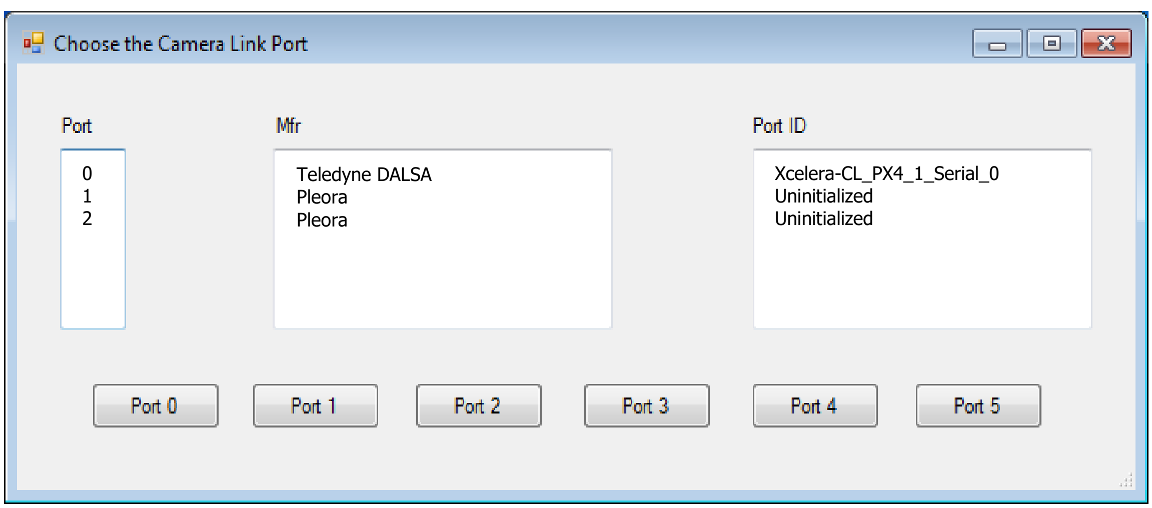
Installation complete.

Note: A shortcut to the program will be placed on the desktop.

Power up the camera and run the Opto Engineering Camera Serial Communication Software.

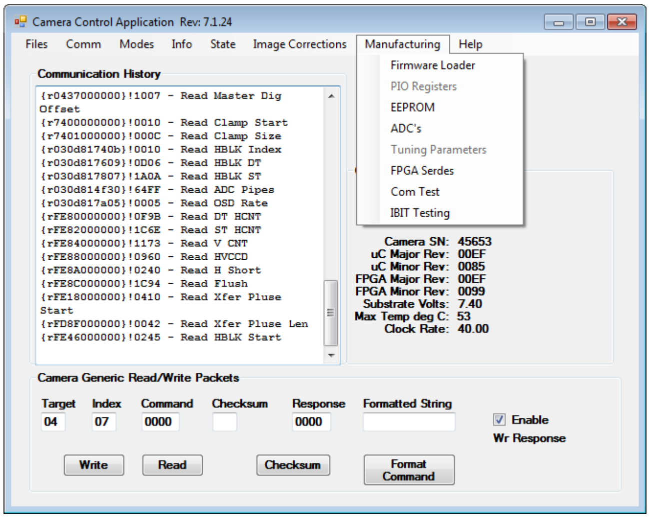
If there are multiple clserxxx.dll's for multiple cards installed, a choice of possible connections will be presented.

If there is only a single capture board present and one clserxxx.dll, the application will simply connect to that card/port.



Getting Started Camera Link

Opto Engineering Camera Serial Communication Software Main

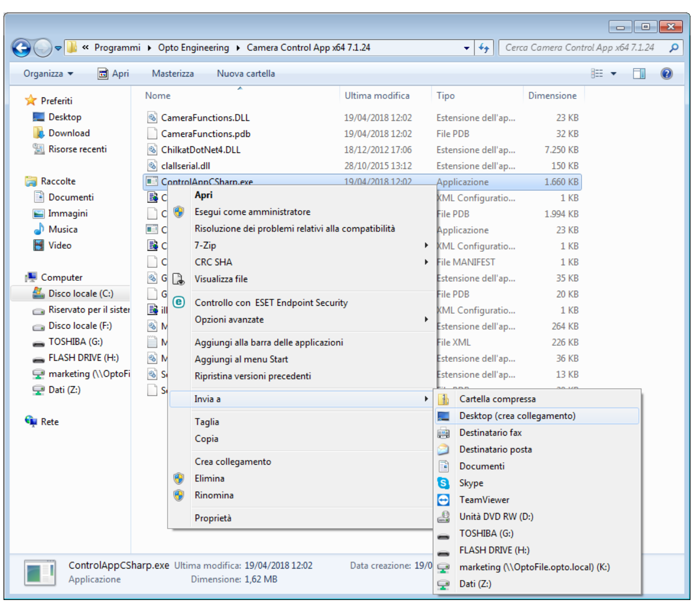


Disabled Menus

By default, sensitive menu items are disabled to prevent inadvertent changes to the camera state. To enable them, a new shortcut has to be created on the desktop.

First, delete the desktop shortcut created by the installer.

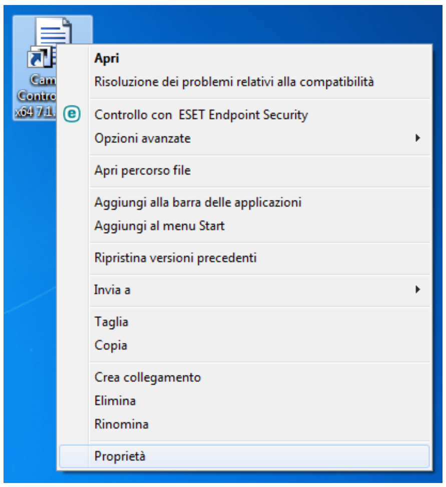
Creating a new shortcut for program options:



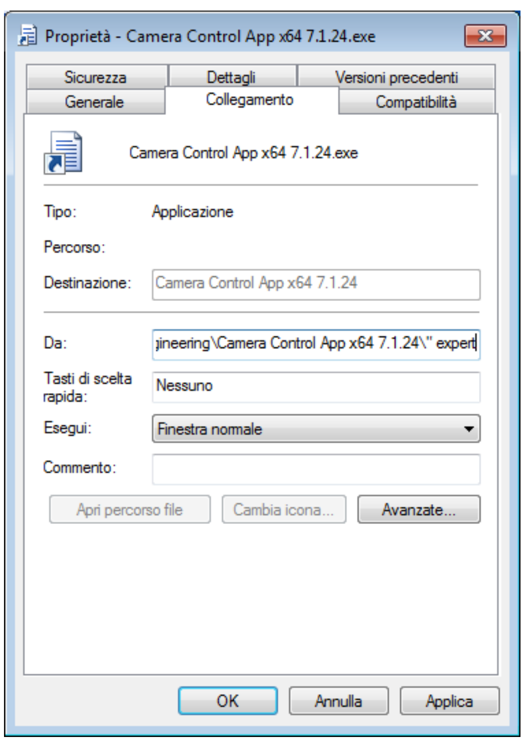
Create a new Shortcut

Navigate to the program install directory and right click on the file with the OE icon and extension .exe. Choose -> Send to -> Desktop. This creates a new desktop shortcut icon.

Adding options to the shortcut command line:



Right click on the newly created desktop icon and select Properties.

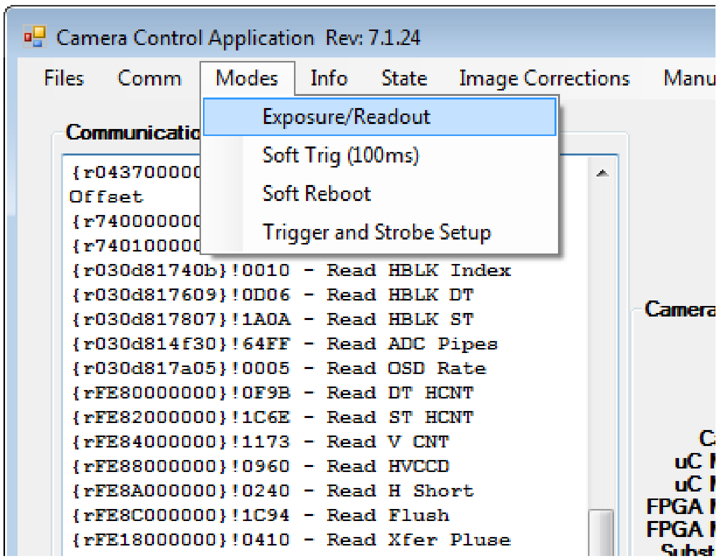


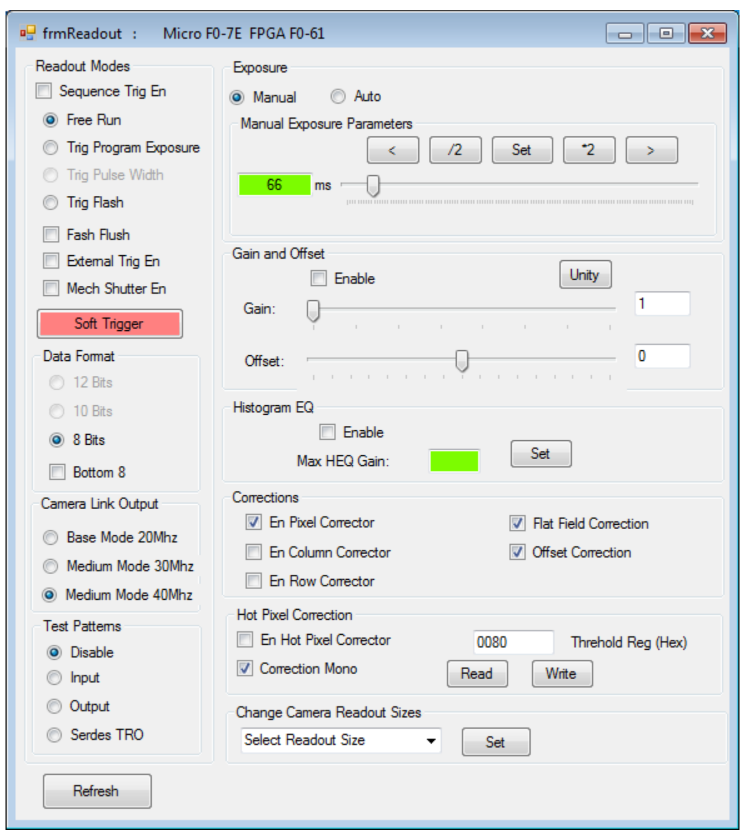
Add a space and the word **expert** after the close quote on the Target: line of the dialog box: .exe" expert

Choose OK.
When the program is launched, all menus will be enabled. **NOTE: Use care with all menus enabled as some changes cannot be undone and may require the camera be returned to the factory for remedy.**

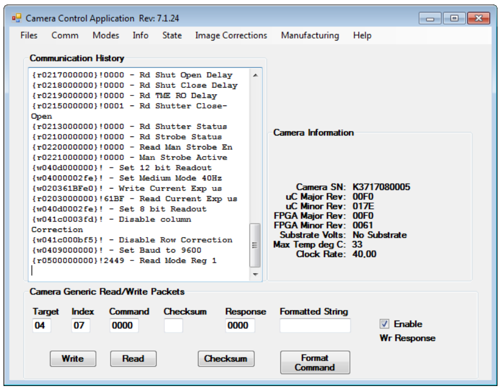
Exposure / Readout:

Start with this dialog box.





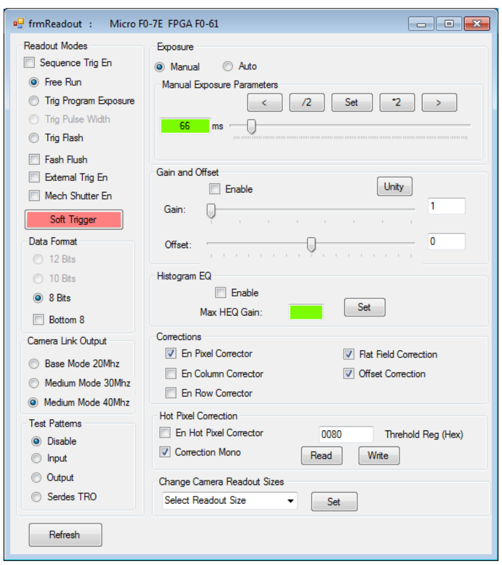
Camera Control Application Details:



Main Dialog

The main dialog box provides access to the various functions of the camera. Menus are used to access sub-dialogs. A generic camera register read/write feature is provided.

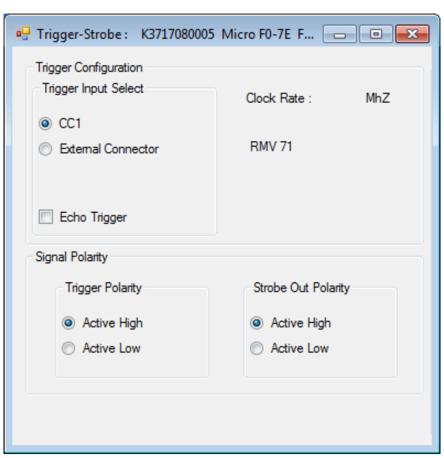
In addition, a history of communication is also provided in this dialog box.



Modes->Exposure and Readout

This dialog box is used to set the Readout Mode, Free Run, or Trigger, as well as the bit depth and exposure of the camera. In addition, the user can set the Camera Link mode, test patterns, digital gain and offset, and histogram equalization.

Pre-defined windowing modes can be selected. A reset (Enable TG) is available.

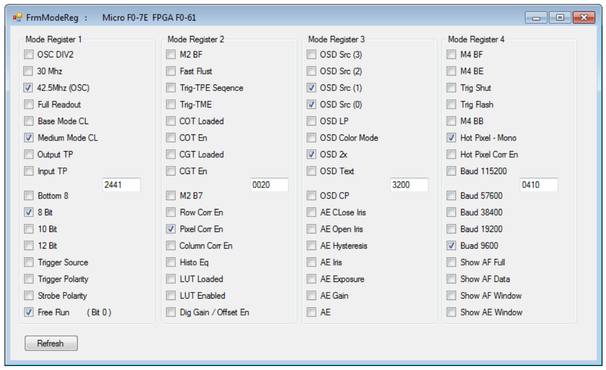


Trigger and Strobe Setup

This dialog box is used to set the trigger source and polarity. The strobe output is only available in the Trigger Exposure Mode.

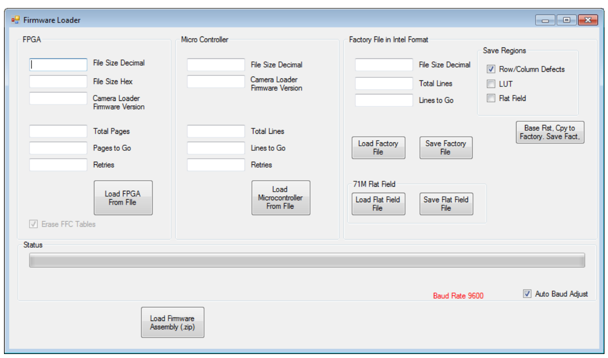
Getting Started Camera Link

Camera Control Application Details:



Mode

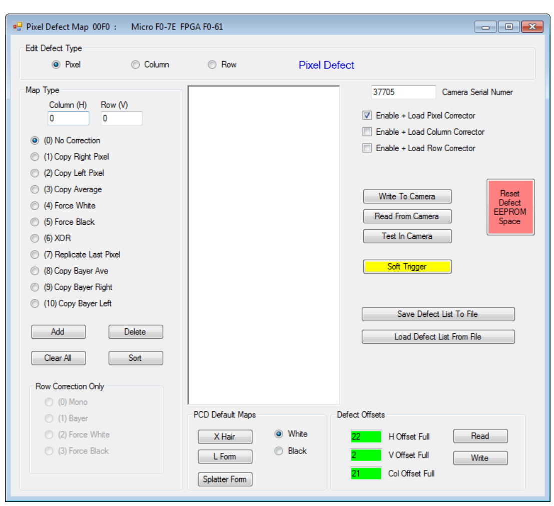
The mode dialog indicates the current mode that the camera is in.



Firmware Loader

The firmware loader dialog is used to load FPGA and Micropro-cessor code as well as the EEPROM configuration data.

A useful feature of this dialog is the ability to save and re- store the camera to and from a file. If there are problems with the camera, the camera state may be saved to a file and then emailed to Opto Engineering for support.



Defect Corrector Editor

The defect corrector editor dialog pro-vides editing of the defect corrector tables.

General Comments:

The control application is for communication with the camera until the user application takes over these functions. All buttons and sliders show the command that is being executed in the application main window.

In the main window, there is a generic read and write section allowing any command that can be found in the manual to be sent to the camera and see its response.

NOTE: If a camera mode is changed, the corresponding change in the capture environment will have to be made as they are independent.

Getting Started USB3

Camera Power
6-12V DC Power to the Hirose 6 pin connector.
Mating Connector: Hirose HR10A-7P-6P

View from Camera Back

USB3 Port
The USB camera connection requires a USB 3.0 compliant hardware port. The camera will not function connected to a USB 2.0 hardware port.

Imaging SDK
Opto Engineering cameras utilize Pleora embedded USB3 hardware inside the camera. The imaging application/SDK are available to download from:

https://supportcenter.pleora.com/s/topic/0TO340000004X6dGAE/ebus-sdk?tabset-25adb=81d66&tabset-0c866=2

Go to downloads to select and download the current viewer for your environment.

USB3 Cables

Opto Engineering recommends CBUSB3001 cables:
https://www.opto-engineering.com/products/CBUSB3001

Camera Communication Software

Opto Engineering Camera Serial Communication Software (GUI)
Download at:
https://www.opto-engineering.com/products/coe-area-scan#Downloads

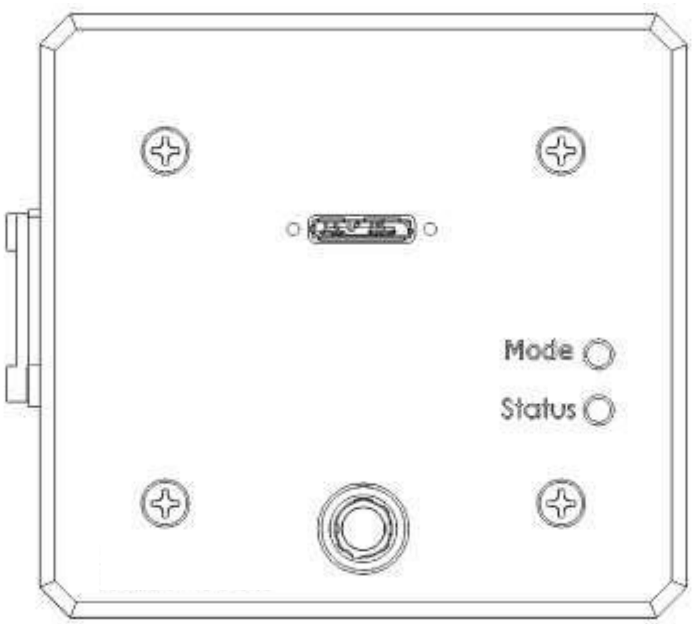
Getting Started USB3

To start imaging with the COE-71 USB3:

Install eBus SDK software software.

Connect the COE-71 USB3 cable to the camera and PC.

Connect the power cable to the camera and apply power.



To start imaging with the CMV-71:

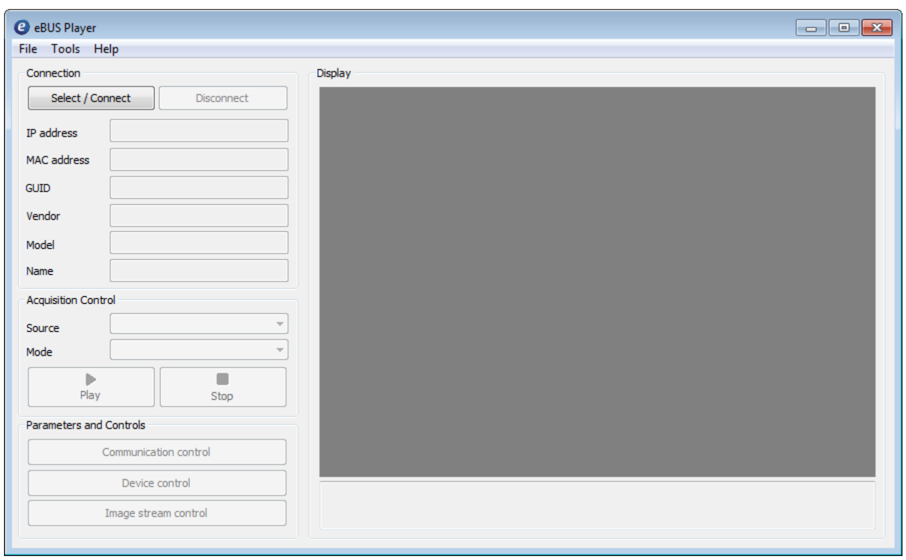
Install eBus SDK software

Additional SDK documentation and resources are available from:
https://supportcenter.pleora.com/s/topic/0TO340000004X6dGAE/ebus-sdk?tabset-25adb=d1819&tabset-0c866=2&tabset-3b862=2

Additional eBus Player documentation and resources are available from:
https://supportcenter.pleora.com/s/topic/0TO34000000PW53GAG/ebus-player?tabset-25adb=70906&tabset-ec78c=2

Install the Opto Engineering Camera Serial Communication Software. Follow the installation instructions beginning on page 7 of this manual, then return here prior to running the camera control application.

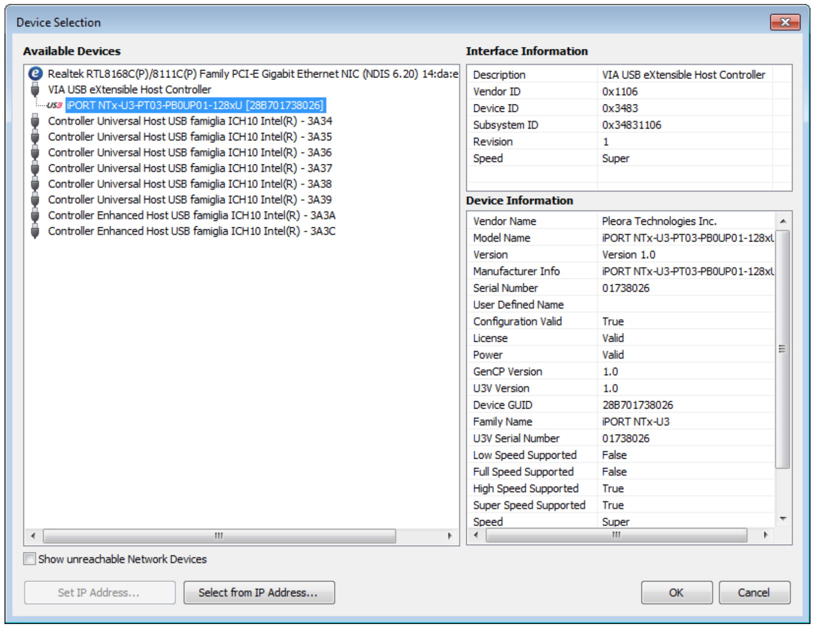
To begin imaging, launch the eBus player.



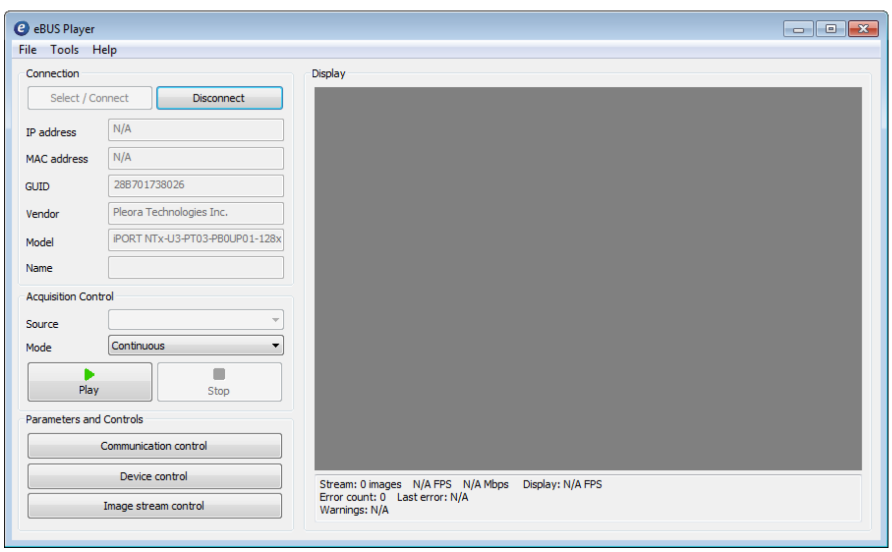
Press Select/Connect

Getting Started USB3

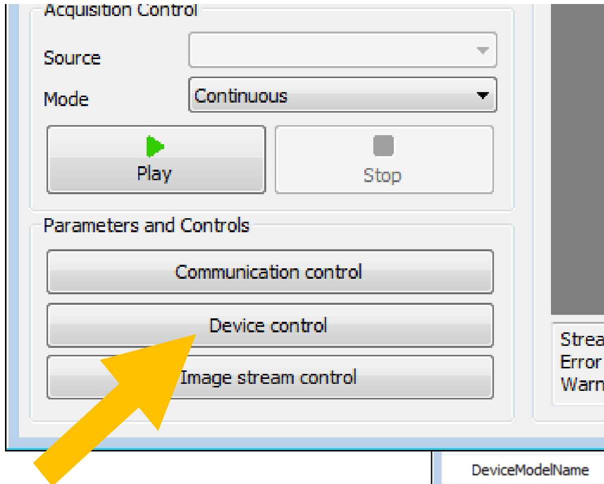
Select the camera and press OK



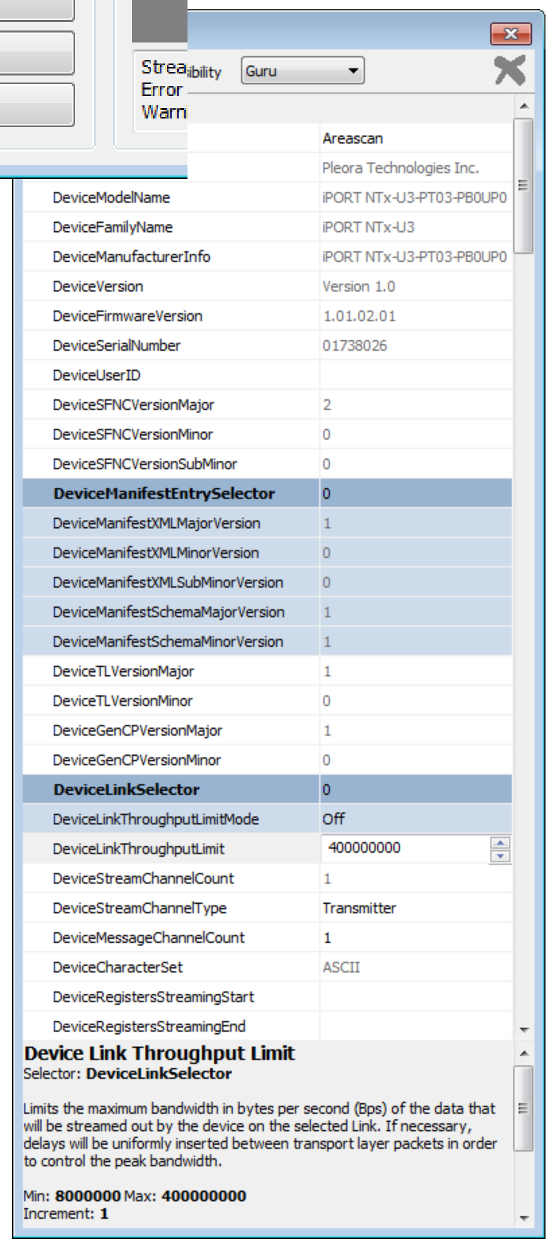
eBus Player is ready to image



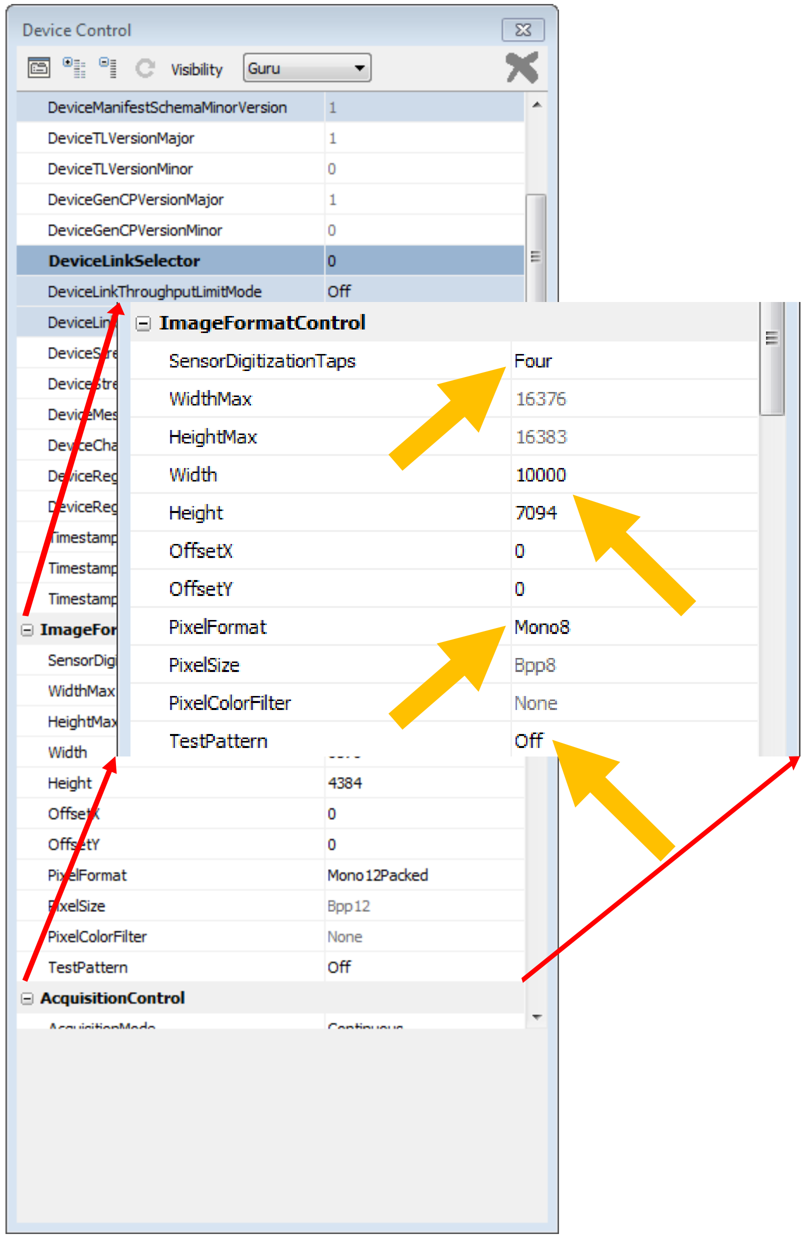
Configure the player:



Select Device Control



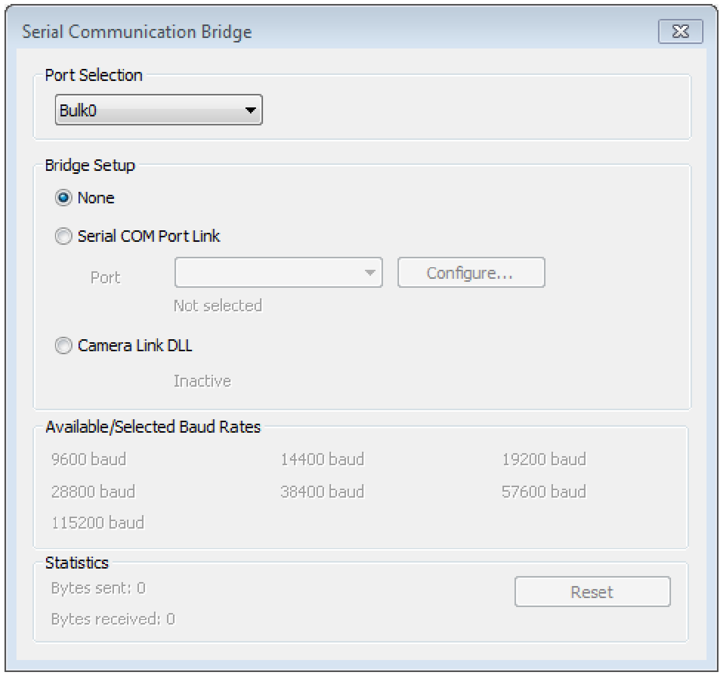
Getting Started USB3



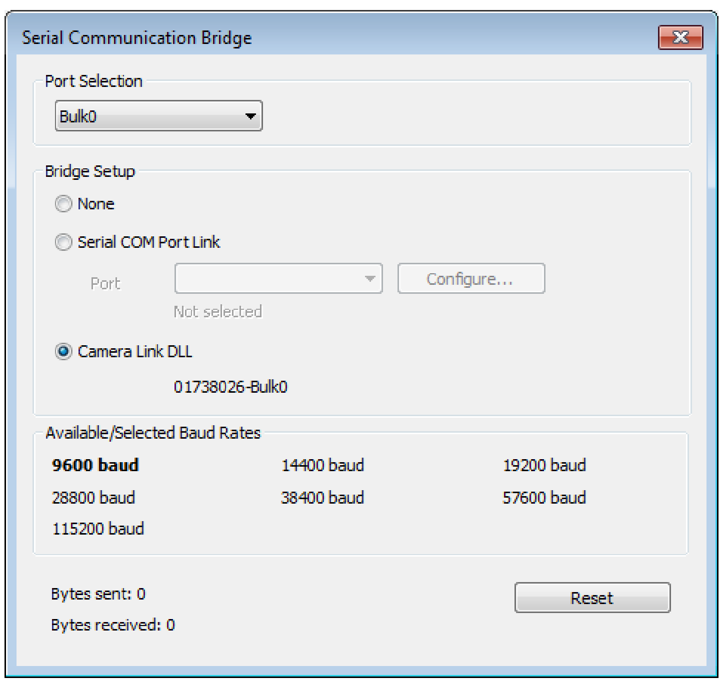
Set the Device Control parameters

Set the raster to **Width** = 10,000 , **Height** = 7094
Turn the **TestPattern** = off
Set the **SensorDigitationTaps** = **Two** or **Four**
Set the **PixelFormat** = **Mono8** or **Mono12Packed**

Getting Started USB3

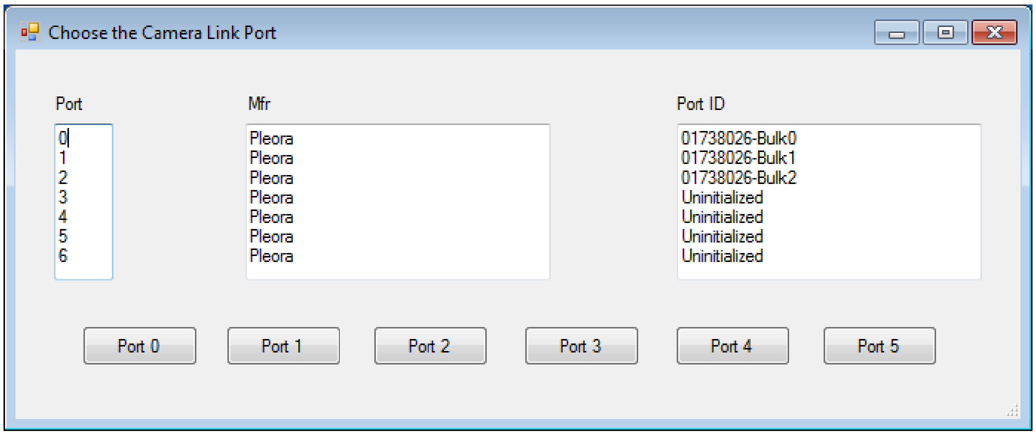


From the Tools Menu on the viewer, choose Serial Communication Bridge

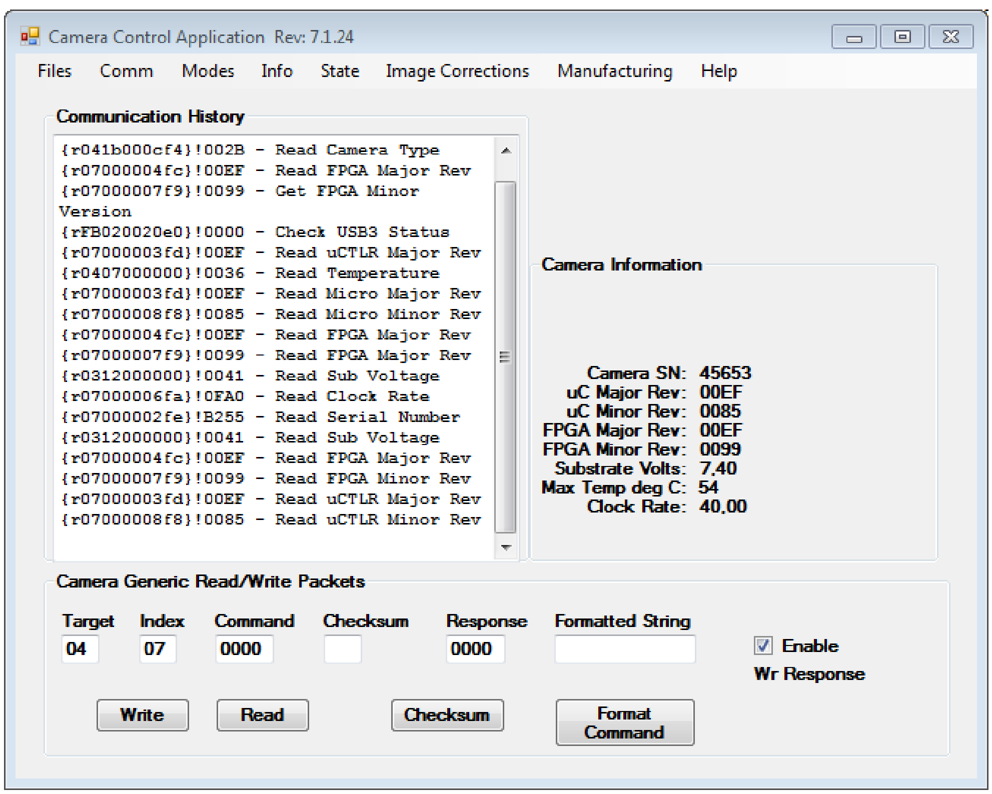


Choose Camera Link DLL - **THEN LEAVE THIS WINDOW OPEN**

Run the Opto Engineering Camera Serial Communication Software that was installed previously:

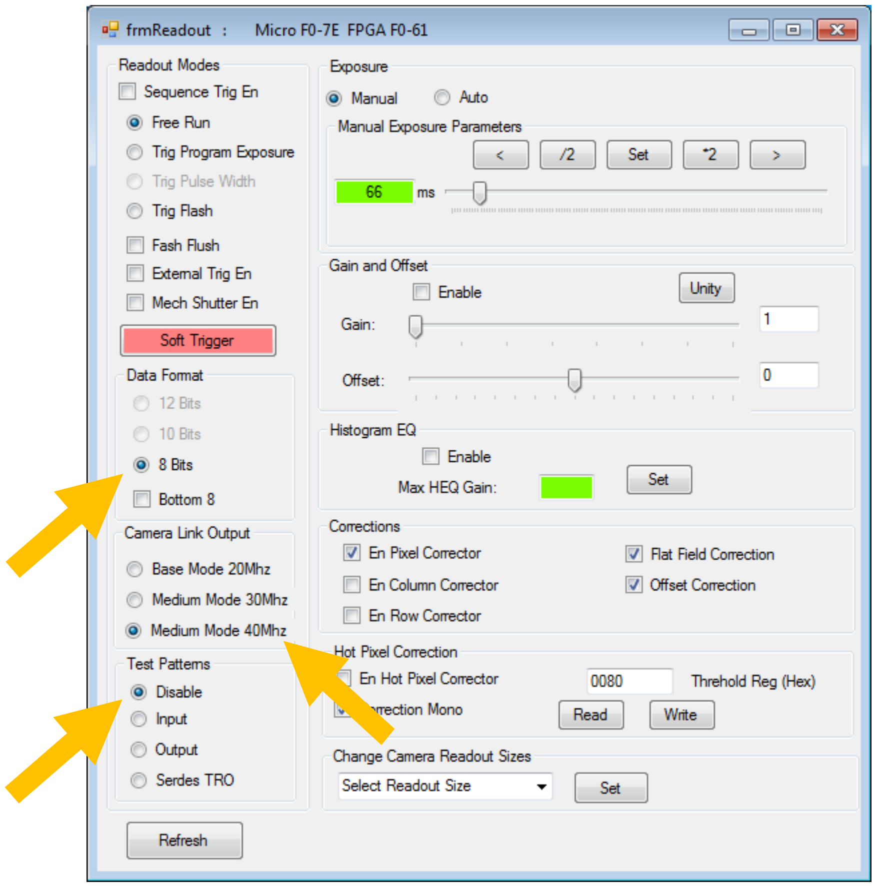


Choose the **BULK0** Interface



The camera serial communication software main window will appear.

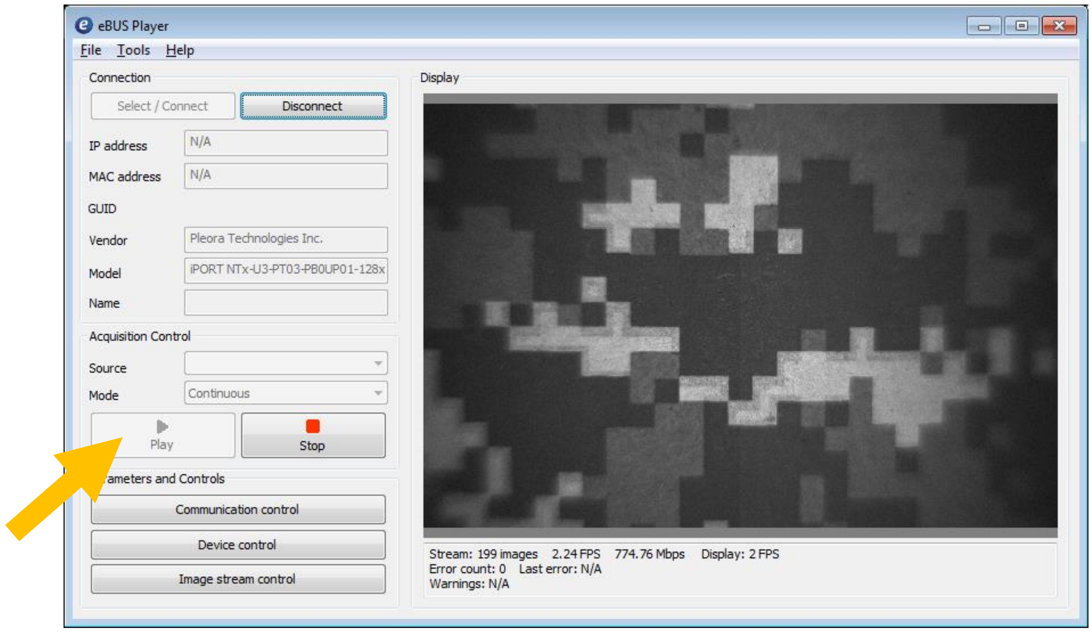
From the **Modes** menu choose Exposure/Readout



Choose the same settings that were set in the Player Device Control earlier.

For the COE-71 the following rates apply

Select **Base Mode 20Mhz** and Data format = **12Bits** or **8Bits**
Select **Medium Mode 30Mhz** and Data format = **8Bits** for 3fps
Select **Medium Mode 40Mhz** and Data format = **8Bits** for 4.2fps



General Comments:

The control application is for communication with the camera until the user application takes over these functions. All buttons and sliders show the command that is being executed in the application main window.

See the Getting Started Camera Link section for more camera control application dialog box documentation.

In the main window, there is a generic read and write section allowing any command that can be found in the manual to be sent to the camera and see its response.

NOTE: If a camera mode is changed, the corresponding change in the eBus Player will have to be made as they are independent.

COE-71 Specifications:

Item	COE-71
Active Image	10,000 x 7096 (Windowing optional)
Sensor Type	ams/CMOSIS CHR71M
Pixel Size	3.1µm x 3.1µm
Sensor Output	8 taps
Video Output	8/10/12 bits
Output Format	Mono or Bayer
Camera Interface	Base or Medium Format Camera Link, USB3
Electronic Shutter	Rolling shutter with Global reset
CL Data rate	2.11 fps (Base CL), 3.0/4.22 fps (Medium CL)
USB3 Data rate	2.11fps 12bit, 3.0/4.22fps 8 bit
Pixel Clock	21.25/30/42.5Mhz
Shutter Speed	Increments of line time.
Windowing	H increments of 16 columns, V increments of 8 rows
Black Level	Adjustable
Analog Gain	1X ~40X
Digital Gain	1X-16X (1/4096 step)
Exposure Modes	Programmed Free Run, Programmed Triggered
External Trigger	3.3-5.0V TTL
Software Trigger	Per Camera API
Dynamic Range	64dB
Defect Correction	Pixel + Column + Row + Hot Pixel
Flat Field Correction	Column Gain, Tap offset
Lens Mount	OEM/M58, Nikon F
Power - varies with mode and data interface	6-14V DC, Max 8W Base Mode ex. ~4.4W @ 12VDC Medium Mode ex. 30Mhz ~5.4W @ 12 VDC Medium Mode ex. 42.5 Mhz ~6.4W @12 VDC
Environmental	Operating 0C to 60C, Storage –40C to +85C
Vibration/Shock	10G (20-200Hz) XYZ 70G 10ms

COE-71 Sensor Specifications:

The COE-71 Digital Camera incorporates the ams/CMOSIS CHR71M-sensor.

Sensor Features

- 10,000 x 7096 active pixels with a 3.1µm pitch.
- Frame rate at full resolution is 4 frames /sec.
- Windowing capability in 16 x 8 pixel increments.
- Moving window capability.
- Selectable pixel clock from two sources (30, 42.5Mhz).
- 8 analog outputs digitized to 12 bits.
- On chip timing for Free Run and Trigger Modes.
- Mono or Bayer pattern output.
- Mono is available as High Grade (No row or column defects)

Sensor Specifications

- Full well charge: > 13ke.
- Sensitivity: 0.15A/W (@ 555nm).
- Dark Noise: 7e-
- Conversion factor: ~63uv/e.
- Dynamic range: 64dB.
- Dark Current: 3.2e-/s @ room temperature.
- Fixed Pattern noise: 0.09 (% of full swing).

Camera - Overview

COE-71 Sensor Pixel Response:

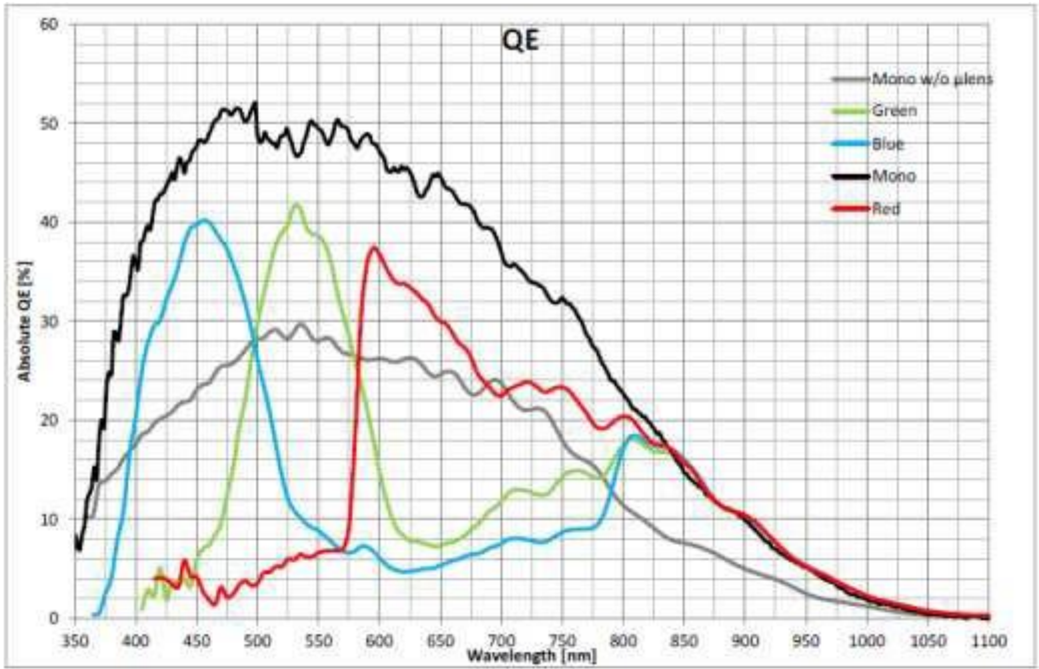


Figure 21: Typical QE of a CHR70M

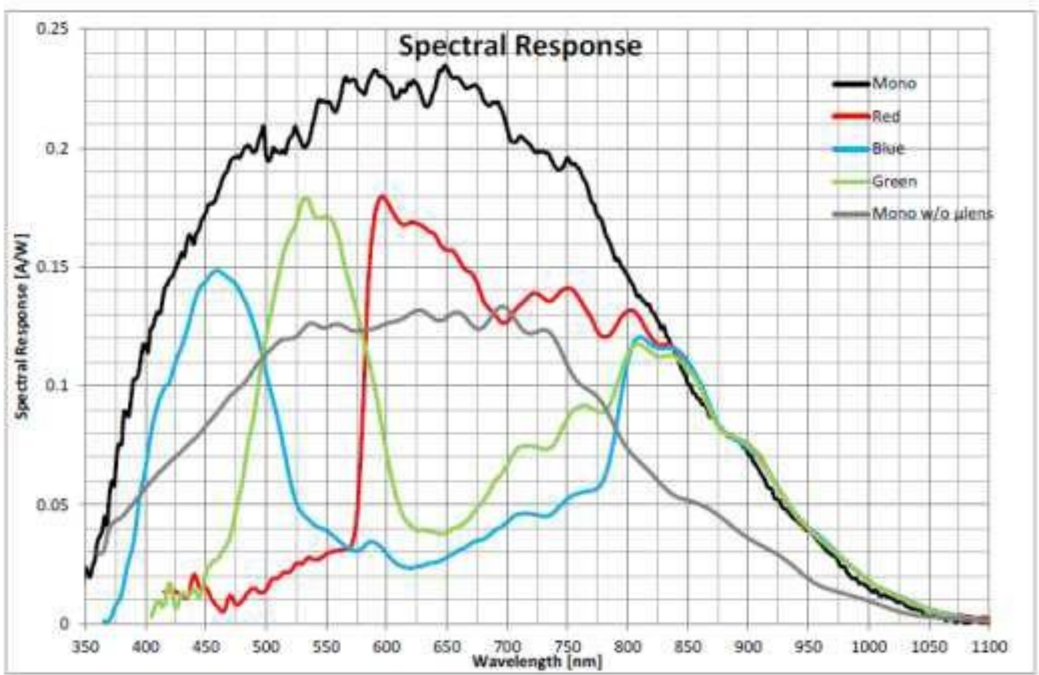
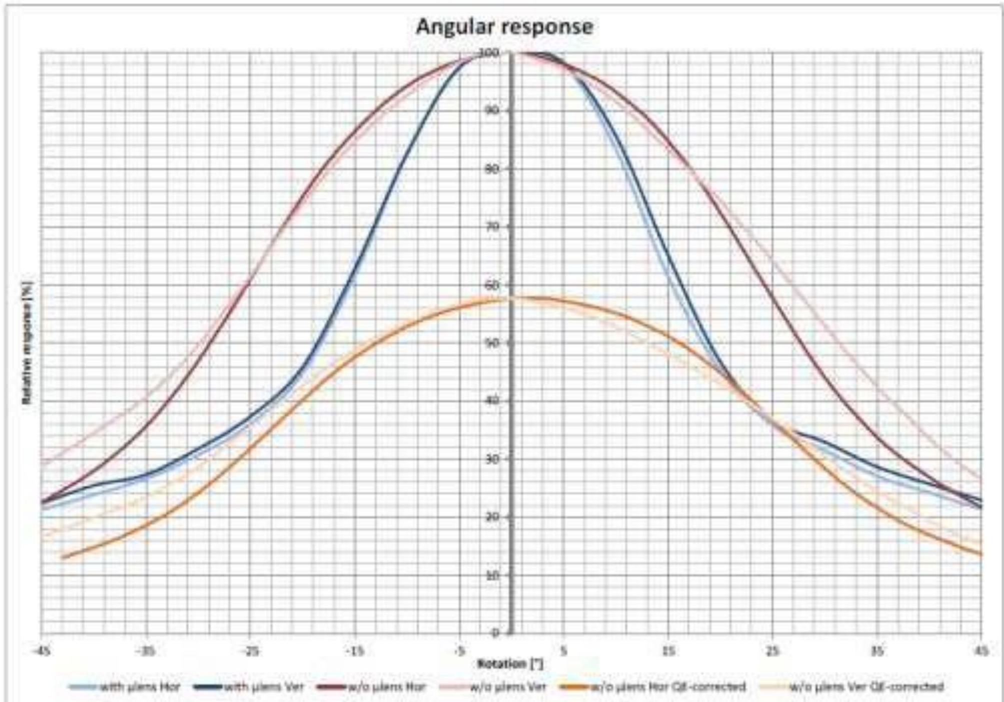
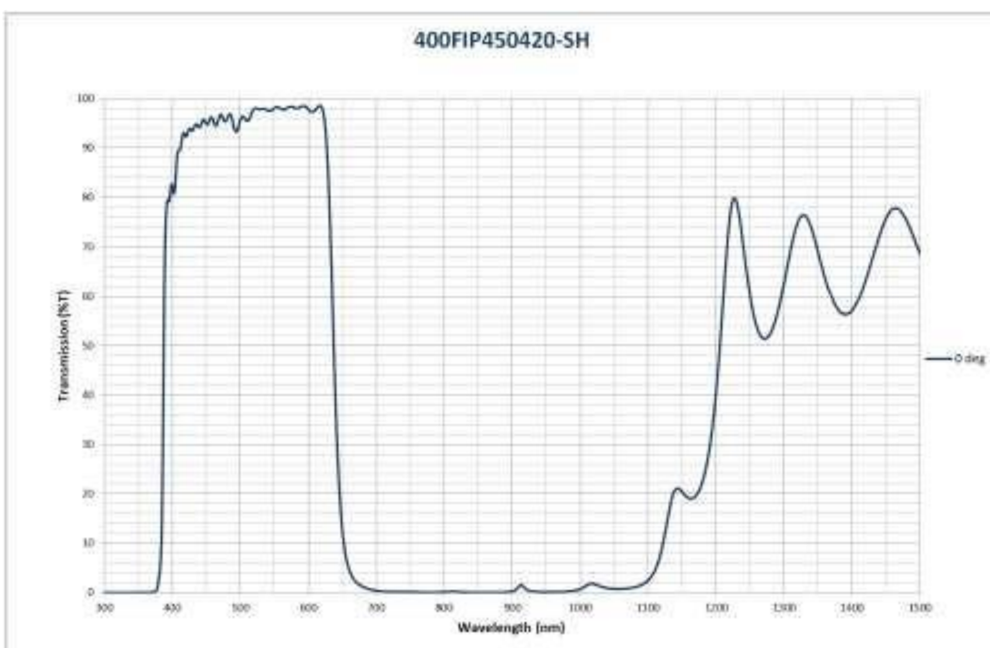


Figure 22: Typical spectral response of a CHR70M

COE-71 Sensor Microlens Angular Response:

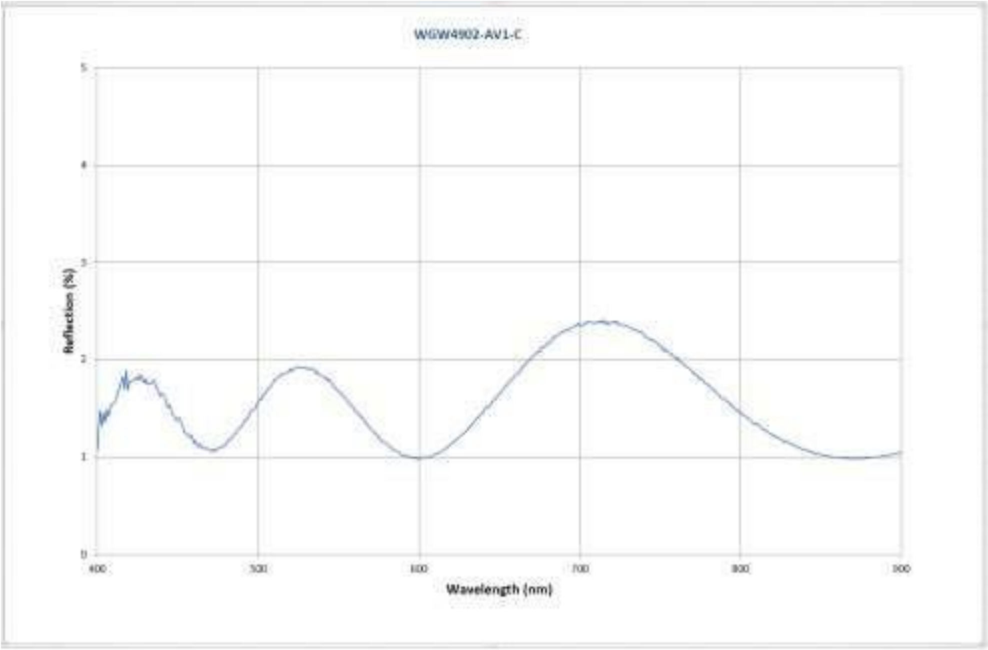


COE-71 IR/UV Filter response:



Camera - Overview

COE-71 Skylight Filter response:



Camera - Overview

Camera - Overview

COE-71 Sensor Pixel Defects - Standard Grade Sensor:

The COE-71 camera uses the ams/CMOSIS CHR71M sensor. The Standard grade sensor can have the following maximum allowable defects:

FPN:	Max 2% RMS
PRNU:	Max 5% RMS
Defective Columns:	15*
Defective Rows:	15*
Defective Pixels:	5000
Clusters 2 pixels:	50
Clusters 3 pixels	20
Clusters 4 pixels	5

*No adjacent column or row defects are allowed.

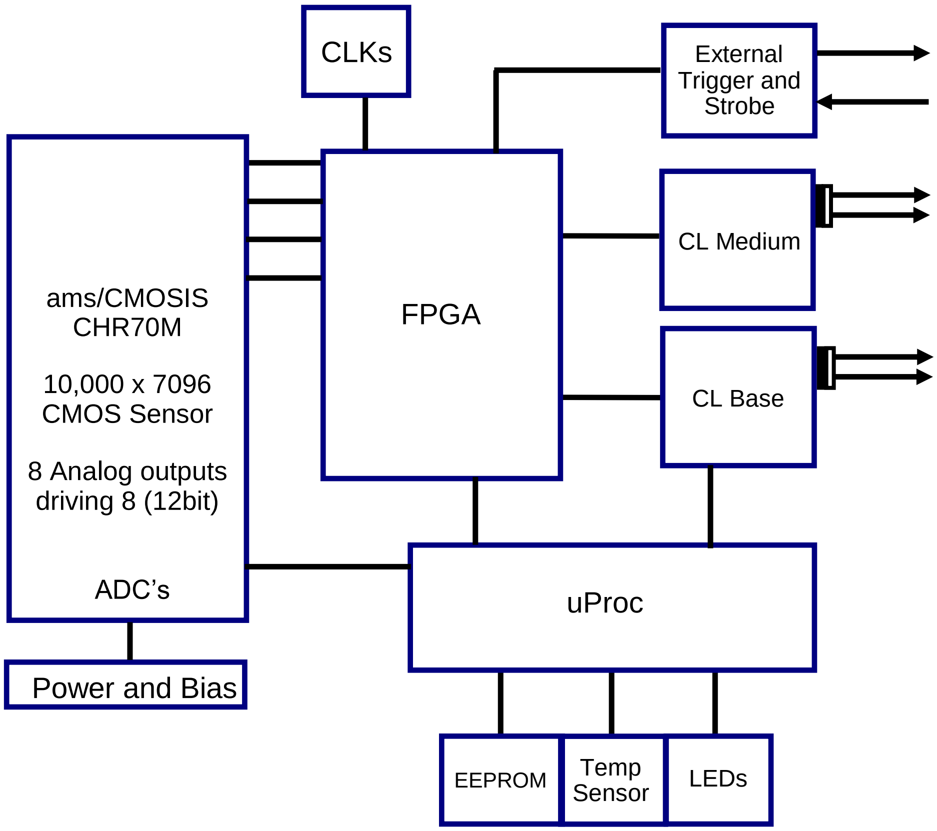
COE-71 Sensor Pixel Defects - High Grade Sensor:

The COE-71 camera uses the ams/CMOSIS CHR71M sensor. The High grade sensor can have the following maximum allowable defects:

FPN:	Max 2% RMS
PRNU:	Max 5% RMS
Defective Columns:	0
Defective Rows:	0
Defective Pixels:	5000
Clusters 2 pixels:	50
Clusters 3 pixels	20
Clusters 4 pixels	5

NOTE:
Defects are corrected in the camera hardware as part of the manufacturing process.

71 Camera Link output block diagram:



The sensor output data is 8 analog taps. Each tap is digitized with an analog to digital converter (ADC) with 12 bit precision. Each ADC is programmable in gain, offset, data phase, and sensing phase (typically the user never has to adjust the ADC).

The FPGA reorders the tap data into two paths of pixels (odd and even) and outputs the pixels onto a Camera Link bus. The output data can be formatted to Camera Link Base Mode (2 (12 bit) pixels per clock) or Camera Link Medium Mode (4 (12 bit) pixels per clock). The Camera Link interface includes trigger and serial communications.

In addition, an external trigger and strobe are provided on the power connector.

The on-board microprocessor controls the sensor and FPGA operation, as well as monitors the various sensors within the camera.

Note: In the case of USB3, the FPGA data is output directly to the USB3 interface board.

Camera Link

Camera Link is a communication interface for visual applications that use digital imaging. The Camera Link (CL) interface is built upon the National Semiconductor Channel Link technology and specifies how image data is formatted and transferred. Channel Link consists of a driver and a receiver pair. The driver accepts 28 single ended data signals and a single ended clock. The data is serialized 7:1 and the four data streams and a dedicated clock are transmitted over five LVDS pairs. The receiver accepts the four data streams and the clock, decodes the data, and drives the 28 bits of data to the capture circuit.

Image data and image enables are transmitted on the Camera Link bus. The four Enable signals are:

FVAL: Frame Valid is defined HIGH for valid lines.
LVAL: Line Valid is defined HIGH for valid pixels.
DVAL: Data Valid is defined HIGH for valid data.
SPARE: undefined, for future use.

Four LVDS pairs are reserved for general purpose camera control. They are defined as camera inputs and frame grabber outputs. The signals are CC1, CC2, CC3, CC4. The CMV-71 uses CC1 as the trigger source.

The Camera Link interface has three configurations:

Base:	Single Channel Link chip, single cable connector.
Medium:	Two Channel Link chips, two cable connectors.
Full:	Three Channel Link chips, two cable connectors.

Note: COE-71 can operate in a **Base** or **Medium** Cameral Link configuration.

COE-71 Performance Camera Link:

The COE-71 is user selectable in Base and Medium Format Camera Link outputs:

Base Mode is limited to 2 channels of data at 85Mhz = 170Mpix/s.
Medium Mode outputs 4 channels of data at 85Mhz = 340Mpix/s.

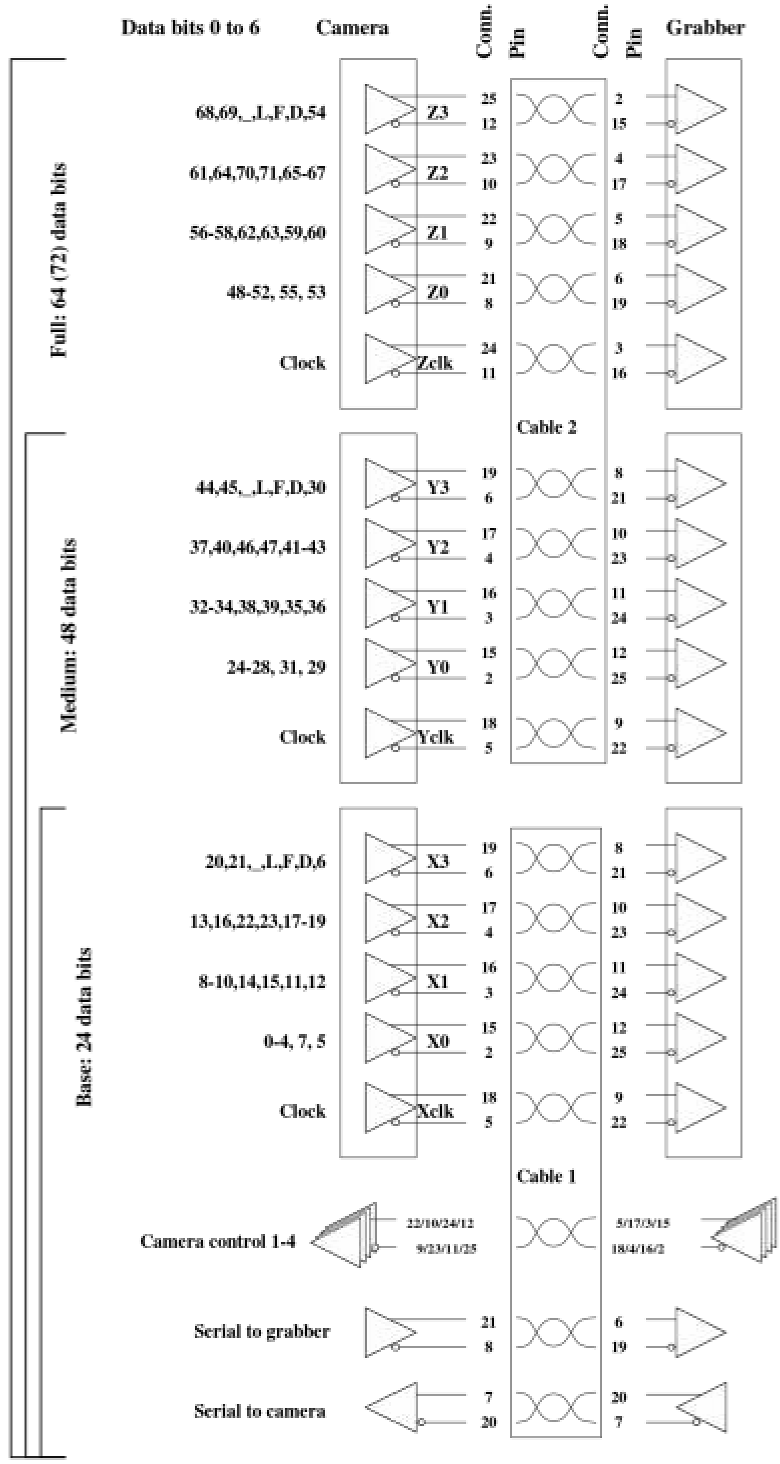
Medium Mode can be selected to run at manufactures specified speed of 30Mhz per tap giving a clock rate of 60Mhz and a full frame rate of ~3 fps.

Medium Mode can also be selected to run at an overclocked speed of 42.5 Mhz per tap giving a clock rate of 85Mhz and a full frame rate of ~4 fps.

All data rates can be output as 8, 10, or 12 bits per pixel.

Camera - Overview

Camera Link



Pixel Format

The COE-71 camera samples the sensor with 12 bit precision and processes the data throughout the FPGA at 12 bits.

During the data format stage, the 12 bit image data can be down sampled to 10 or 8 bits. In addition, the bottom 8 bit data can be output as the top 8 (msb) of the 12 bit image sample.

Sensor ADC pixel sample to Camera Link mapping			
ADC bits	12 bit CL	10 bit CL	8 bit CL
11	11>11	11>9	11>7
10	10>10	10>8	10>6
9	9>9	9>7	9>5
8	8>8	8>6	8>4
7	7>7	7>5	7>3
6	6>6	6>4	6>2
5	5>5	5>3	5>1
4	4>4	4>2	4>0
3	3>3	3>1	
2	2>2	2>0	
1	1>1		
0	0>0		

Channel Format

The Camera Link Base Mode used on the CMV-71 camera, can transfer pixel data in 8, 10, 12 bit depths and in one or two channels. Two channel mode allows for a transfer clock frequency 1/2 of the single channel mode.

The Camera Link Medium Mode transfers four pixels per clock. The Medium Mode requires two Camera Link cables and a capture card that is compatible with the Medium format.

COE-71 ROI Frame Rate Table Camera Link:

CMV-71 Base	Full	4HD	2HD	HD	VGA
SensorX	10000	7680	3840	1920	640
SensorY	7096	4320	2160	1080	480
ROT clks	168	168	168	168	168
ClockMhz	**21.25**	**21.25**	**21.25**	**21.25**	**21.25**
Taps	8	8	8	8	8
LineTime us	66.73	53.08	30.49	19.20	11.67
FrameTime ms	473.5	229.3	65.9	20.7	5.6
Frames fps	**2.11**	**4.36**	**15.18**	**48.23**	**178.51**

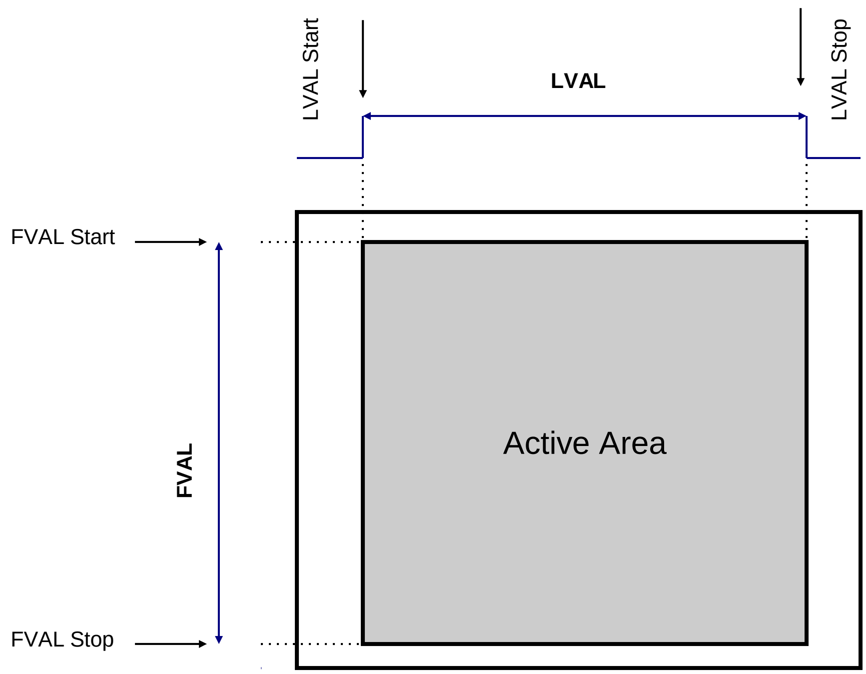
CMV-71 Medium CL	Full	4HD	2HD	HD	VGA
SensorX	10000	7680	3840	1920	640
SensorY	7096	4320	2160	1080	480
ROT clks	168	168	168	168	168
ClockMhz	**30**	**30**	**30**	**30**	**30**
Taps	8	8	8	8	8
LineTime us	47.27	37.60	21.60	13.60	8.27
FrameTime ms	335.4	162.4	46.7	14.7	4.0
Frames fps	**2.98**	**6.16**	**21.43**	**68.08**	**252.02**

CMV-71 Medium CL Max	Full	4HD	2HD	HD	VGA
SensorX	10000	7680	3840	1920	640
SensorY	7096	4320	2160	1080	480
ROT clks	168	168	168	168	168
ClockMhz	**42.5**	**42.5**	**42.5**	**42.5**	**42.5**
Taps	8	8	8	8	8
LineTime us	33.36	26.54	15.25	9.60	5.84
FrameTime ms	236.8	114.7	32.9	10.4	2.8
Frames fps	**4.22**	**8.72**	**30.36**	**96.45**	**357.02**

Camera - Overview

Camera Link Valids

The COE-71 camera samples and processes the entire area of the image sensor. In the standard operating mode, only the active image area is output on the Camera Link as valid data. The LVAL/FVAL signals, which define the valid pixel data, can be programmed to output any part of the image, including the optical black clamping areas. FVAL start/stop are specified in lines. LVAL start is in pixels plus the overhead of the CCD vertical clocks. LVAL stop is specified as the same as LVAL start with the exception of its maximum value of 1. VALID start and stop changes are not stored on system save and must be reprogrammed each time they are needed.



Target	Index	Command	R/W	Description
0x04	0x1b	System Registers	R	0x0008 = LVAL Start 0x0009 = LVAL Stop 0x000a = FVAL Start 0x000b = FVAL Stop
0x04	0x27	System Registers	W	0x0008 = LVAL Start 0x0009 = LVAL Stop 0x000a = FVAL Start 0x000b = FVAL Stop

See the section 'Serial Communication' for the use of these commands

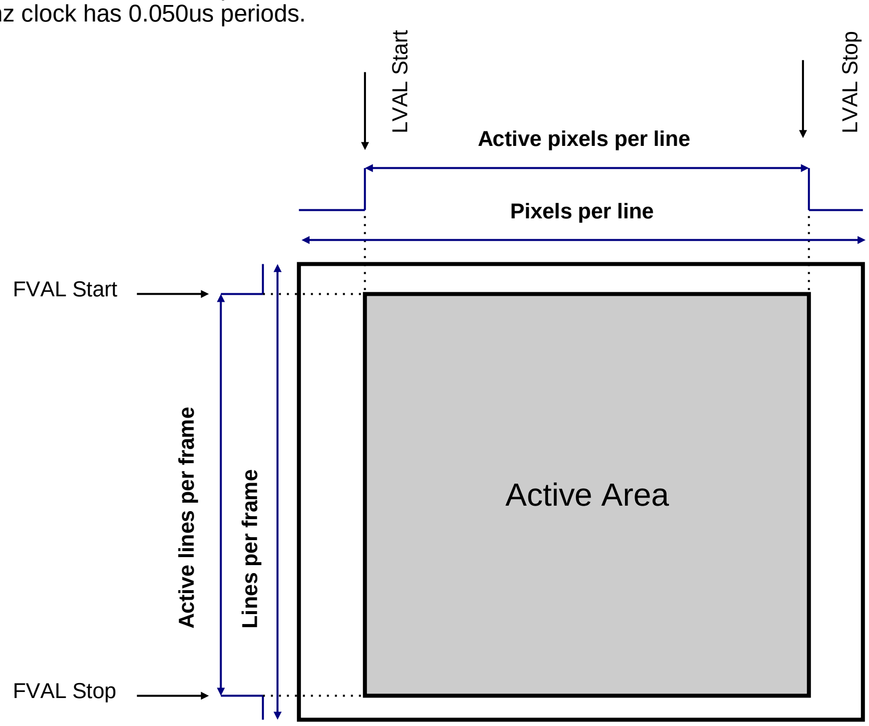
Channel Format

The COE-71 can generate many different raster formats. To document all possible combinations of binning, partial scan, and triggering is next to impossible; therefore, to alleviate this problem the COE-71 incorporates a set of Raster Detectors that measure the video image raster as sent to the capture device. These measured values can be used to set the capture parameters. In addition to the raster size, an Exposure Detector is included. The Exposure Detector measures the exposure of the CCD sensor in units of the master pixel clock rate. The frame CRC is used in the Built-in-test functions of the camera.

Target	Index	Command	R/W	Description
0x04	0x1b	System Registers	R	0x0000 = Pixels per line 0x0001 = Active pixels per line 0x0002 = Lines per frame 0x0003 = Active lines per frame 0x0012 = Exposure counter low word 0x0013 = Exposure counter high word 0x0014 = Frame CRC

See the section 'Serial Communication' for the use of these commands

NOTES
- ►Active pixels per line = LVAL active pixel count.
- ►Active lines per frame = FVAL active line count.
- ►The Exposure Detector counter is a 32 bit integer. This gives a range of exposure from one clock period to over 2 seconds.
- ►Exposure is measured in pixel clock periods.
  A 40Mhz clock has 0.025us periods.
  A 30Mhz clock has 0.033us periods.
  A 20Mhz clock has 0.050us periods.



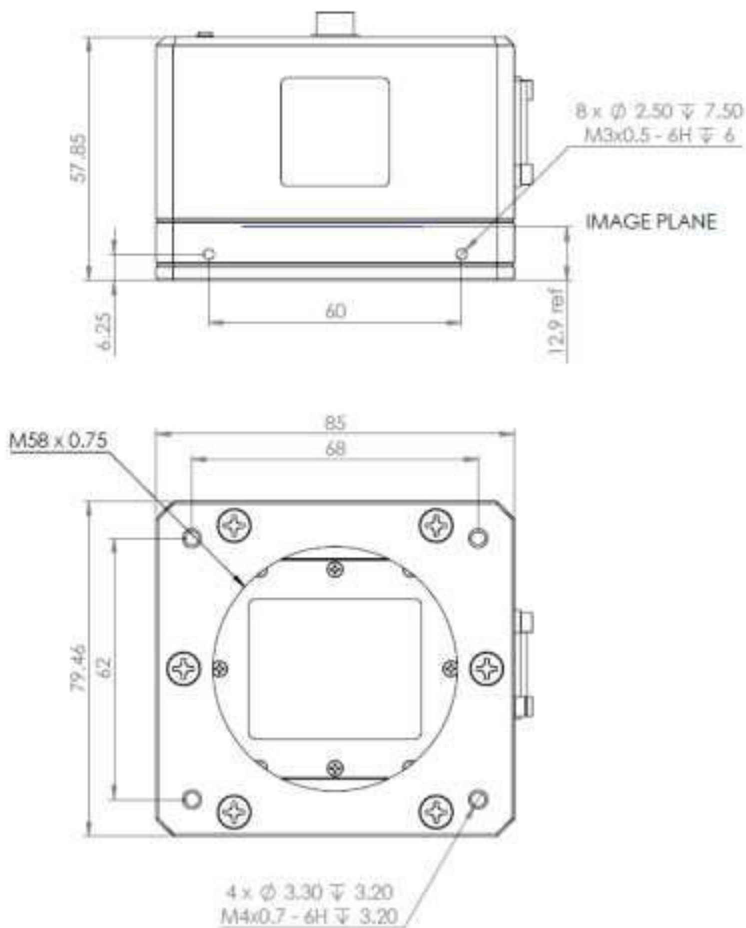
Camera - Overview

Drawings and CAD Models:

The COE-71 case dimensions are available on the Opto Engineering web site under the camera and interface of interest. See the web page for the most current mechanical drawings.

CAD Models are available at https://www.opto-engineering.com.

USB3

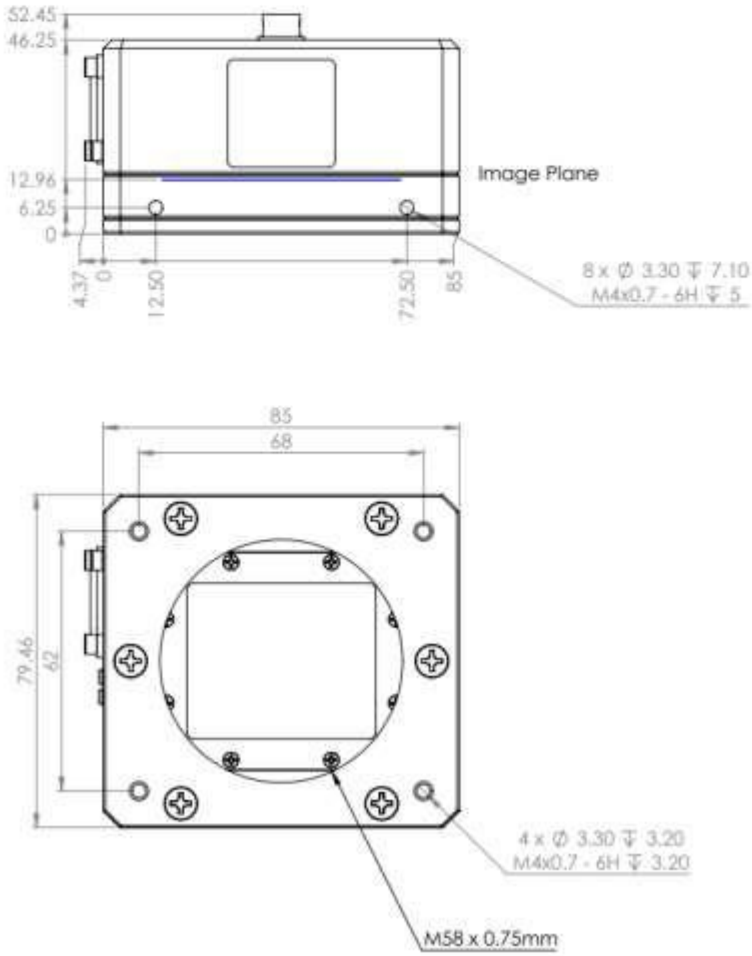


Lens Interfaces:

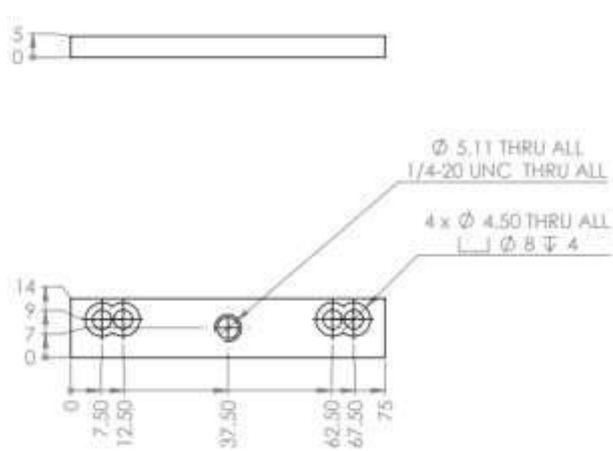
The COE-71 base configuration for all data interfaces is an M58/OEM mount. Optional mounts include Nikon F.

Hardware Overview

Camera Link

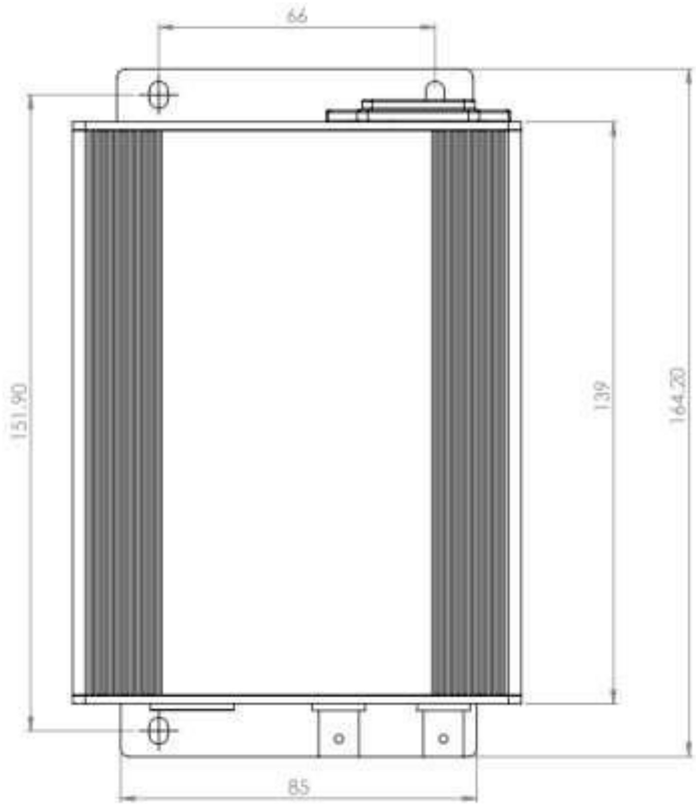


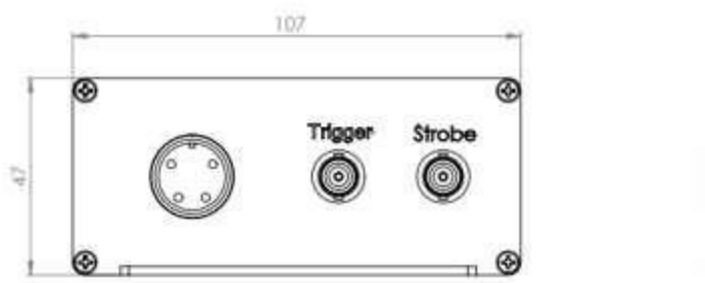
Tripod Adapter



Hardware Overview

12V Universal Power Supply





The COE-71 serial interface was developed for high reliability applications. The interface incorporates error checking and a handshake protocol, which responds with either a positive or negative acknowledge signal. The communication path from frame grabber to the COE-71 is through the Camera Link cable. The Camera Link committee has specified that devices connected must first communicate at 9600 baud, but the COE-71 has a selectable baud rate for faster communication speeds.

The COE-71 microprocessor is a flash programmable device with many features vital to the operation of the camera. Some of these features include:

- Hardware UART used for serial communications.
- A watchdog timer used to monitor communication errors and system faults.
- Onboard RAM and EEPROM for saving camera settings.
- Parallel data bus for high speed interfaces to the FPGA and NAND FLASH memories.
- Brown out detection and reset.

SERIAL INTERFACE PROTOCOL

Implementation

Camera communication is accomplished via asynchronous serial communication according to EIA Standard RS 232 C through the Camera Link cable.

Data rate: Full Duplex, 9600 baud.

- 1 START bit.
- 8 DATA bits – The LSB (D0) is transfered first.
- 1 STOP bit.
- No parity.

Protocol

The COE-71 camera is controlled through command packets. The COE-71 camera is considered a slave device and never generates data without a read request. The data packet formatting is described in detail below. ***Note:*** the checksum is calculated only on the 4 ascii characters comprising the Data.

Data Packets

Data packets are of either 'read' or 'write' types. For example: to read the camera serial number, the packet sent to the camera would be {r07000002fe}. The camera would respond by issuing an acknowledge character ! followed by the response {r0700sssscc}, where ssss is the camera serial number and cc is the checksum calculated in hex as 0x0100 – (ss (high byte hex) + ss (low byte).

Packet Format							
1 Char	2 Char	2 Char	2 Char	4 Char	2 Char	1 Char	1 Char
Start	**Command**	**Target**	**Index**	**Data**	**Checksum**	**End**	**Ack/ Nack**

Start: Indicates the Start of the frame
Size = 1 ascii character
Value = 123 Decimal (ascii {)

Command:
Command descriptor
Size = 1 ascii character
Value = 114 Decimal (ascii r) for Read
Value = 119 Decimal (ascii w) for Write

Target:
Command descriptor
Size = 2 ascii characters

Index:
Command descriptor
Size = 2 ascii characters

Data:
The data transferred
Size = 4 ascii characters

Checksum of Data
Size = 2 ascii characters - Intel-Standard - two's compliment of sum of data.

Example 1: Data = 2002, checksum = lower byte of (0x100 – (0x20 + 0x02)) = 0xde
Example 2: Data = 0000, checksum = lower byte of (0x100 – (0x00 + 0x00)) = 0x00
Example 3: Data = fef0, checksum = lower byte of (0x100 – (0xfe + 0xf0)) = 0x12

End:
Indicates the End of the frame
Size = 1 ascii character
Value = 125 Decimal (ascii })

Ack/Nack:
Positive **Ack**nowledge - **N**egative **ack**nowledge
Size = 1 ascii character
Ack Value = 33 Decimal (ascii !)
Nack Value = 63 Decimal (ascii ?)

COMMAND DESCRIPTIONS

Read Command Structure

The COE-71 camera parses the sequence byte by byte. An invalid read command, target , or index will cause the camera to issue a NACK. The Host (the user) will generate dummy data with a valid checksum then an end. The camera will respond with an ACK and re-send the command with valid data and checksum. If the Host detects an error, it will re-issue the command.

Host {r tt ii 0 0 0 0 cc}, camera issues !
Camera issues {r tt ii data data data data cc} (NOTE no ACK).

Write Command Structure

The COE-71 camera parses the sequence byte by byte. An invalid write command, target, index, or checksum will cause the camera to issue a NACK; otherwise, the write sequence will complete and the camera will issue an ACK after the command has been executed. The camera receives the checksum from the Host.

Host {w tt ii data data data data cc} camera issues !

Error Checking

The COE-71 camera parser is character by character and will respond with an immediate NACK if any unrecognized command, target, index, or checksum occurs.

Communication Timeouts

The COE-71 camera micro-controller uses a hardware watchdog timer that will time out if the time between bytes are longer than 500ms. When sending command frames to the camera, the host must not have significant delays between bytes sent.

Camera Control

Target	Index	Description	Read Write	Modes
0x04	0x00	CL Format	W	0x0000 = Camera Link Base 0x0001 = Camera Link Medium 0x0002 = Camera Link Medium overclock
0x04	0x03	Trigger Mode Select	R/W	0x0000 = Free Run 0x0001 = Trigger Program Exposure 0x0009 = Trigger Source CL 0x000a = Trigger Source External
0x5C	0x10	Window Y Start	R/W	Location in pixels, will be rounded to nearest 8th row.
0x5C	0x11	Window X Start	R/W	Location in pixels, will be rounded to nearest 16th column.
0x5C	0x12	Window Y Stop	R/W	Location in pixels, will be rounded to nearest 8th row.
0x5C	0x13	Window X Stop	R/W	Location in pixels, will be rounded to nearest 16th column.
0x5E	0x00	Full Readout	W	Sensor 10,000x7096 output
0x5E	0x01	Pre-set Window	W	Window 1920x1080 in center of sensor
0x5E	0x02	Pre-set Window	W	Window 3830x2160 in center of sensor
0x5E	0x03	Pre-set Window	W	Window 640x480 in center of sensor
0x5E	0x04	Pre-set Window	W	Window 7680x4320 in center of sensor
0x5E	0x05	Pre-set Window	W	Window 256x256 in center of sensor
0x5E	0x06	Pre-set Window	W	Window 1024x1024 in center of sensor
0x5E	0x07	Pre-set Window	W	Window 2048x2048 in center of sensor
0x5E	0x08	Pre-set Window	W	Window 4096x4096 in center of sensor
0x5E	0x09	Pre-set Window	W	Window 7096x7096 in center of sensor
0x5E	0x0A	Pre-set Window	W	Window 10000x1080 in center of sensor
0x5E	0x80	Set Window Readout	W	Must setup X/Y Size as below
0x5E	0x81	Set Window X Size	W	Sets width of centered window
0x5E	0x82	Set Window Y Size	W	Sets height of centered window
0x60	0x00	Low Noise Function	W	Stops internal sensors
0x60	0x01	Normal Function	W	Restores all functionality

Target	Index	Description	Read Write	Modes
0x04	0x06	Test Pattern	W	0x0000 = Normal Video 0x0001 = FPGA Input Test Pattern 0x0002 = Output Test Pattern
0x04	0x07	Camera Temperature	R	
0x04	0x09	Baud Rate	W	0x0000 = 9600 0x0001 = 19200 0x0002 = 38400 0x0003 = 57600 0x0004 = 115200
0x04	0xD2	Set Camera Link Boot Baud Rate (Requires reboot)	R/W	0x0000 = 9600 0x0001 = 19200 0x0002 = 38400 0x0003 = 57600 0x0004 = 115200
0x04	0x1c	Defect Correction (DC)	W	0x0000 = Load/Enable Pixel DC 0x0001 = Load/Enable Column DC 0x000A = Load/Enable Row DC 0x0005 = Disable Pixel DC 0x0004 = Disable Column DC 0x000B = Disable Row DC
0x04	0xA0	Hot Pixel Corrector	R/W	0x0000 = Disabled 0x0001 = Enabled
0x04	0xA1	Hot Pixel Correction Type	R/W	0x0000 = Color Bayer 0x0001 = Monochrome
0x04	0xA2	Hot Pixel Threshold	R/W	Threshold in dn
0x04	0xA3	# Hot pixels corrected	R	In # pixels * 256 (0x0001 = 256 cor.)
0x04	0x24	Digital Gain	R/W	In units of 1/4096 gain Example 0x1000 = 1X gain 0xC800 = 12.5X gain
0x04	0x30	Digital Offset	R/W	Signed value 0x0100 = offset of +256 0xFEFF = offset of –255
0x04	0x38	Digital Gain/Offset Enable	R/W	1 = enable, 0 = disable
0x04	0x0d	Bit Depth	W	0x0000 = 12 bit mode 0x0001 = 10 bit mode 0x0002 = 8 bit mode 0x0003 = Enable bottom 8 bits 0x0004 = Disable bottom 8 bits
0x04	0x0e	Strobe Control	W	0x0000 = negative strobe polarity 0x0001 = positive strobe polarity

Target	Index	Description	Read Write	Modes
0x04	0x1b	System Registers	R	0x0000 = Read Pixels/Line 0x0001 = Read Active Pixels/Line 0x0002 = Read Lines per frame 0x0003 = Read Active Lines per frame 0x0008 = LVAL Start 0x0009 = Stop 0x000a = FVAL Start 0x000b = Stop 0x000d = FPGA Revision 0x0012 = Read Exposure value low 0x0013 = Read Exposure value high 0x0014 = Read CRC
0x04	0xFF	Base Reset	W	Resets camera mode to: free run no LUT, no PDC, no digital gain or offset, no test pattern, reset the LVAL and FVAL defaults. enable strobe in Free Run Mode
0x04	0xD8	Checksum Mode (Cleared on re-start)	W	0x0000 = Checksum of data 0x0001 = Checksum of command and data

Exposure Type

The exposure type is either Free Run Mode or Trigger Mode.
In Free Run Mode, the camera outputs continuous images in a rolling shutter mode.
In Trigger Mode, the camera receives the trigger, erases the pixels, exposes the image, and then reads it out.

Target	Index	Description	Read Write	Modes
0x04	0x03	0x0000	W	Set Free Run Mode
0x04	0x03	0x0001	W	Set Trigger Mode
0x5C	0x01	# of frames	W	Set number frames read in Trigger Mode
0x04	0x03	0x0009	W	Set Trigger Source Camera Link
0x04	0x03	0x000A	W	Set Trigger Source power cable (external)

Exposure Control

The exposure time is set in either milliseconds or microseconds. The resolution of the exposure is in horizontal line times. Two commands are provided for calculating the Free Run time from a specified time variable (milliseconds or microseconds). **The closest available time is selected and set in the internal time variable.**

Target	Index	Description	Read Write	Modes
0x02	0x02	Set Exposure ms	W	Set Exposure time in milliseconds
0x02	0x03	Set Exposure us	W	Set Exposure time in us
0x02	0x02	Get Exposure ms	R	Return actual time in milliseconds
0x02	0x03	Get Exposure us	R	Return actual time in us (0xFFFF = to large).
0x02	0x05	Soft Trigger Time	W	Software trigger in ms 1 - 65535
0x02	0x06	Set Trigger high	W	Sets internal trigger high (active)
0x02	0x07	Set Trigger low	W	Sets internal trigger low

Bit Depth

Target	Index	Description	Read Write	Modes
0x04	0x0d	Output Bit Depth	W	0x0000 = 12 bit mode 0x0001 = 10 bit mode 0x0002 = 8 bit mode 0x0003 = Bottom 8 bits (as Msb)

Strobe Signal

The COE-71 Strobe Signal is a 3.3V LVTTL signal that is active when the sensor is triggered and exposing an image. The Strobe Signal is useful for analyzing and optimizing imaging applications. The strobe can be used to activate an illumination source. If used in this fashion, the Strobe Signal cannot drive significant current and should be buffered.

Target	Index	Description	Read Write	Modes
0x04	0x0e	Strobe Control	Write	0x0000 = negative strobe polarity 0x0001 = positive strobe polarity

Memory Management

Target	Index	Description	Read Write	Modes
0x03	0x00	Save Camera State	W	Wait for acknowledge before removing power.
0x03	0x00	Save Camera State in Background	W	Returns immediately, operates in background.
0x03	0x02	Restore Factory State	W	Wait for acknowledge before removing power.
0x03	0x03	Copy User to Factory	W	Wait for acknowledge before removing power.
0x03	0x09	Reset EEPROM CRC	W	
0x03	0x0d	EEPROM Word	R/W	0xaaaa = address Read address directly Write data word to 030c then write 030d with address.
0x03	0x0e	EEPROM Byte	R/W	0xaaaa - address Read address directly Write data byte to 030c then write 030e with address.

System and Status

Target	Index	Description	Read Write	Modes
0x05	0x00	Camera Mode/Status	R	0x0000 = read mode register 1 0x0001 = read mode register 2 0x0002 = read mode register 3 0x0003 = read mode register 4 0x0005 = read status register 1 0x0006 = read status register 2
0x07	0x00	Camera Parameters	R	0x0000 = Camera Model 0x0001 = Camera Hardware Rev 0x0002 = Camera Serial Number 0x0003 = Micro-firmware Rev 0x0004 = FPGA Major Revision 0x0005 = Sensor Serial Number 0x0006 = Clock Rate 0x0007 = FPGA Sub/Minor Revision 0x0008 = Micro Sub/Minor Revision 0x0009 = Camera Type 0x000A = FPGA Clk Speed

Times

Target	Index	Description	Read Write	Modes
0x5E	0xD0	Get Line Time	R	Returns line time in us
0x5E	0xD1	Get Frame Time	R	Returns frame time in us
0x5E	0xD2	Get Frame Time	R	Returns frame time in ms

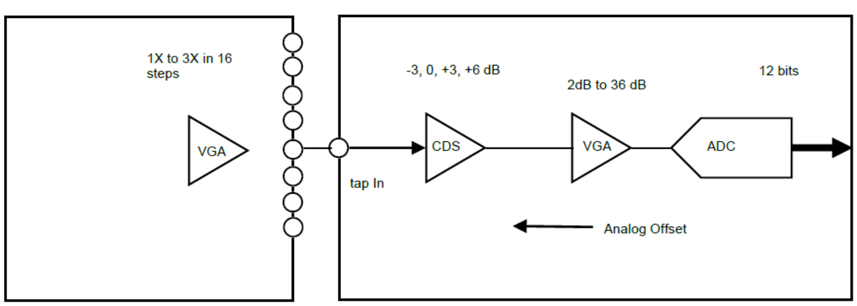
Gains and Offsets

The COE-71 camera has 8 individual analog taps. Each tap is processed by an analog front end (AFE). Each AFE has two gain stages and a 12 bit analog to digital converter. The CMOS Sensor has an additional internal gain stage. This gain is normally set to minimum to reduce system noise.

ADC Gain can be calculated with the following equation.

Gain (dB) = 5.1 + (0.0359 * code)
Where code is the range of 0 to 1023.

Target	Index	Description	Read Write	Modes
0x00	0x00	ADC Gain	W	0x0000-0x3FF Writes all 8 ADC's with gain value
0x00	0x80	Black Level	R/W	Higher value is a darker image
0x00	0x44	Pre (CDS) Gain	R/W	Sets all 8 ADC's
0x5C	0x08	CHR71M Gain	R/W	0x0000-0x000F Write sensor gain



Mode and Status Register Bit Assignments

```
typedef struct                                  // Status Register 1
        {
        unsigned int
        WDT_ENABLED:            1,              //1 = WDT enabled BIT 0
        XIL_CONFIG:             1,              //1 = Xilinx config failed
        BROWNOUT:               1,              //1 = Brownout reset
        PWR_NORMAL:             1,              //1 = Normal power up reset

        WDT_RESET:              1,              //1 = WDT timeout
        UART_ERR:               1,              //1 = UART ERROR
         VSYNC_TIMEOUT:         1,              //1 = VSYNC timeout received
        DCM_TIMEOUT:            1,              //1 = DCM timeout

         HW_DCM_LOCKED:         1,              //1 = DCM Locked
        S1_B9:                  1,              //
        VAFE_ERR:               1,              //1 = AFE 1.8V error
        V3_ERR:                 1,              //1 = 3V Switcher error

        VIN_ERR:                1,              //1 = 12V input error
        V5_ERR:                 1,              //1 = 5V Switcher error
        VF_ERR:                 1,              //1 = FPGA 1.2 or 2.5V Error
        FACT_CRC_ERR:           1;              //1 =

    }status_register1_t;

typedef struct                                  // Status Register 2
        {
        unsigned int
        ADC_VID1_SAVE_FAIL:     1,              //1 = ADC 1 state save fail
        ADC_VID2_SAVE_FAIL:     1,              //1 = ADC 2 state save fail
        ADC_VID3_SAVE_FAIL:     1,              //1 = ADC 3 state save fail
        ADC_VID4_SAVE_FAIL:     1,              //1 = ADC 4 state save fail

        PIO_SAVE_FAIL:          1,              //1 = PIO state save fail
        IBIT1_COMP:             1,              //1 = IBIT1 Complete
        S2_B6:                  1,              //
        S2_B7:                  1,              //

        S2_B8:                  1,
        ADC_VID5_SAVE_FAIL:     1,              //1 = ADC 5 state save fail
        ADC_VID6_SAVE_FAIL:     1,              //1 = ADC 6 state save fail
        ADC_VID7_SAVE_FAIL: 1   ,               //1 = ADC 7 state save fail

        ADC_VID8_SAVE_FAIL:     1,              //1 = ADC 8 state save fail
        S2_NAD:                 1,              //1 =
        AE_ERR:                 1,              //1 =
        USER_CRC_ERR:           1;              //1 =

    }status_register2_t;
```

Serial Commands

```
typedef struct                                  // Mode Register 1 = READOUT
        {
        unsigned int
        free_run:                  1,           // 1 = free run mode 0 = trigger
        strobe_polarity:           1,           // 1 = positive strobe polarity
        trigger_polarity:          1,           // 1 = positive trigger polarity
        trigger_source:            1,           // 0 = CL 1 = External

        twelve_bit:                1,           // 1 = 12 bit readout
        ten_bit:                   1,           // 1 = 10 bit readout
        eight_bit:                 1,           // 1 = 8 bit readout
        bottom_8:                  1,           // 1 = bottom 8 bit readout

        input_TP:                  1,           // 1 = input test pattern enabled
        output_TP:                 1,           // 1 = output test pattern enabled
        Med_mode_readout:          1,           //1 = Medium mode readout (4 tap path)
        Base_mode_readout:         1,           //1 = Base mode readout (2 tap path)

        full_readout:              1,           // 1 = 10,000 x 7096 0 = window
        osc_42mhz:                 1,
        Osc_30mhz:                 1,
        Osc_div2:                  1;
    } mode_register1_t;
typedef struct                                  // Mode Register 2 = Defect and image correction
        {
        unsigned int
        DGO_enabled:               1,           // Master Digital gain and offset
        LUT_enabled:               1,
        LUT_LOADED:                1,           //1 = LUT Loaded from EEPROM
        HISTO_EQ:                  1,           //1 = Histogram equalization enabled

        CDC_EN:                    1,           //1 = Column Defect Corrector Enabled
        PDC_EN:                    1,           //1 = Pixel Defect Corrector Enabled
        RDC_EN:                    1,           //1 = Row Defect Corrector Enabled
        M2_B7:                     1,           //

        CGT_enabled:               1,
        CGT_LOADED:                1,           //1 = Column Gain Table Loaded from EEPROM
        COT_enabled:               1,
        COT_LOADED:                1,           //1 = Column Offset Table Loaded from EEPROM

        M2_BC:                     1,           //
        M2_BD:                     1,           //
        M2_BE:                     1,           //
        M2_BF:                     1;           //
    } mode_register2_t;
typedef struct                                  // Mode Register 3 = Detectors and AE
        {
        unsigned int
        AE:                        1,           //1 = auto exposure enabled
        AE_gain:                   1,           //1 =
        AE_exposure:               1,           //1 = AE in exposure mode
        AE_iris:                   1,           //1 =

        AE_hysteresis:             1,           //1 = AE within hysteresis
        AE_OPEN_IRIS:              1,           //1 = AE at max gain - need more light BIT 0 PRESERVE
        AE_CLOSE_IRIS:             1,           //1 = AE at min exposure - need less light PRESERVE
        OSD_CP:                    1,           //

        OSD_TEXT:                  1,           //1 = OSD text display enabled PRESERVE
        OSD_2X:                    1,           //1 = 2X text box BIT0
        OSD_COLOR_MODE:            1,           //1 = OSD Color Mode
        OSD_LP:                    1,           //

        OSD_SCR:                   4;           //1 = OSD Screen type ( bits)
    } mode_register3_t;
typedef struct                                  // Mode Register 4 = Communication and misc.
        {
        unsigned int
        AE_WINDOW:                 1,           //1 = Show AE Window
        AF_WINDOW:                 1,           //1 = Show AF Window
        AF_DATA:                   1,           //1 = Show AF Data
        AF_FULL:                   1,           //1 = Show AF Data Full Screen

        BAUD_9600:                 1,           //1 = 9600 baud
        BAUD_19200:                1,           //1 = 19200 baud
        BAUD_38400:                1,           //1 = 38400 baud
        BAUD_57600:                1,           //1 = 57600 baud

        BAUD_115200:               1,           //1 = 115200 baud
        HotPixelEnabled            1,           //
        HotPixelMono               1,           //
        M4_BB:                     1,           //

        TriggeredFlash:            1,           //
        TriggeredShutter:          1,           //
        CLK_SEL:                   1,           //
        PowerDown:                 1;           //
    } mode_register4_t;
```

Lookup Tables

Preset LUTs

The camera has some predefined look up tables that may be loaded quickly into the camera with one camera command. The tables and commands are listed below. Once these tables are loaded, the LUT is automatically enabled.

Loading LUT for Use and/or Storage

LUT tables can be created on a PC and loaded into a camera. The Opto Engineering Camera Control Application has a table create feature, a load table into camera RAM and EEPROM (storage), and a load table into camera RAM.

To load tables into the camera or enable a stored table in the camera, the Lut_mode register needs to be set to the desire function.

Target	Index	Description	Read Write	Modes
0x04	0x31	Preset Tables	W	0001 = Linear LUT 0002 = Invert LUT 0003 = Knee LUT 0004 = Gamma 0.45 LUT 0005 = Gamma 0.60 LUT 0006 = Gamma 0.70 LUT 0007 = Gamma 0.80 LUT
0x04	0x46	Load Gamma Table	W	XXXX when XXXX > 0 and XXXX <= 100. Gamma value is xxxx/100
0x04	0x45	Lut_mode	W	0000 = Load LUT From File on PC , No EEPROM Save 0001 = Load LUT From File on PC , EEPROM Save 0002 = Load LUT from EEPROM

Communication BAUD Rates

The Camera Link 1.0 specification allows for serial communication at 9600 baud only. The 1.1 specification (and later) provides for faster rates.

The COE-71 camera allows for the setting of the baud rate to one of five rates. This setting can be made for only the current power cycle or for the boot cycle.

The COE-71 camera allows the user the option of saving the communication speed in the camera EEPROM. This can cause communication with the camera to be lost if the command is not used carefully. ***Note:*** only one of the baud rates will be used so that if communication is lost it can be restored by trying the other baud rates.

Once the EEPROM baud rate is set, the camera must be re-powered to set the rate.

Target	Index	Description	Read Write	Modes
0x04	0x09	Set Current Baud Rate	W	0x0000 = 9600 0x0001 = 19200 0x0002 = 38400 0x0003 = 57600 0x0004 = 115200
0x04	0xD2	Set Camera Link Boot Baud Rate (Requires reboot)	R/W	0x0000 = 9600 0x0001 = 19200 0x0002 = 38400 0x0003 = 57600 0x0004 = 115200
0x04	0xD3	External Serial Boot Baud Rate (Requires reboot)	R/W	0x0000 = 9600 0x0001 = 19200 0x0002 = 38400 0x0003 = 57600 0x0004 = 115200
0x04	0xD0	Power Up	W	Resets camera and powers up circuits

Serial Commands

Windowed Readout

The Windowed Readout command changes the raster readout of the CHR71M sensor. Window sizes are rounded to 16 pixels horizontally and 8 pixels vertically.

Target	Index	Description	Read Write	Modes
0x5C	0x10	Window Y Start	R/W	Location in pixels, will be rounded to nearest 8th row.
0x5C	0x11	Window X Start	R/W	Location in pixels, will be rounded to nearest 16th column.
0x5C	0x12	Window Y Stop	R/W	Location in pixels, will be rounded to nearest 8th row.
0x5C	0x13	Window X Stop	R/W	Location in pixels, will be rounded to nearest 16th column.
0x5E	0x00	Full Readout	W	Sensor 10,000x7096 output
0x5E	0x01	Pre-set Window	W	Window 1920x1080 in center of sensor
0x5E	0x02	Pre-set Window	W	Window 3830x2160 in center of sensor
0x5E	0x03	Pre-set Window	W	Window 640x480 in center of sensor
0x5E	0x04	Pre-set Window	W	Window 7680x4320 in center of sensor
0x5E	0x05	Pre-set Window	W	Window 256x256 in center of sensor
0x5E	0x06	Pre-set Window	W	Window 1024x1024 in center of sensor
0x5E	0x07	Pre-set Window	W	Window 2048x2048 in center of sensor
0x5E	0x08	Pre-set Window	W	Window 4096x4096 in center of sensor
0x5E	0x09	Pre-set Window	W	Window 7096x7096 in center of sensor
0x5E	0x0A	Pre-set Window	W	Window 10000x1080 in center of sensor
0x5E	0x80	Set Window Readout	W	Must setup X/Y size as below
0x5E	0x81	Set Window X size	W	Sets width of centered window
0x5E	0x82	Set Window Y size	W	Sets height of centered window

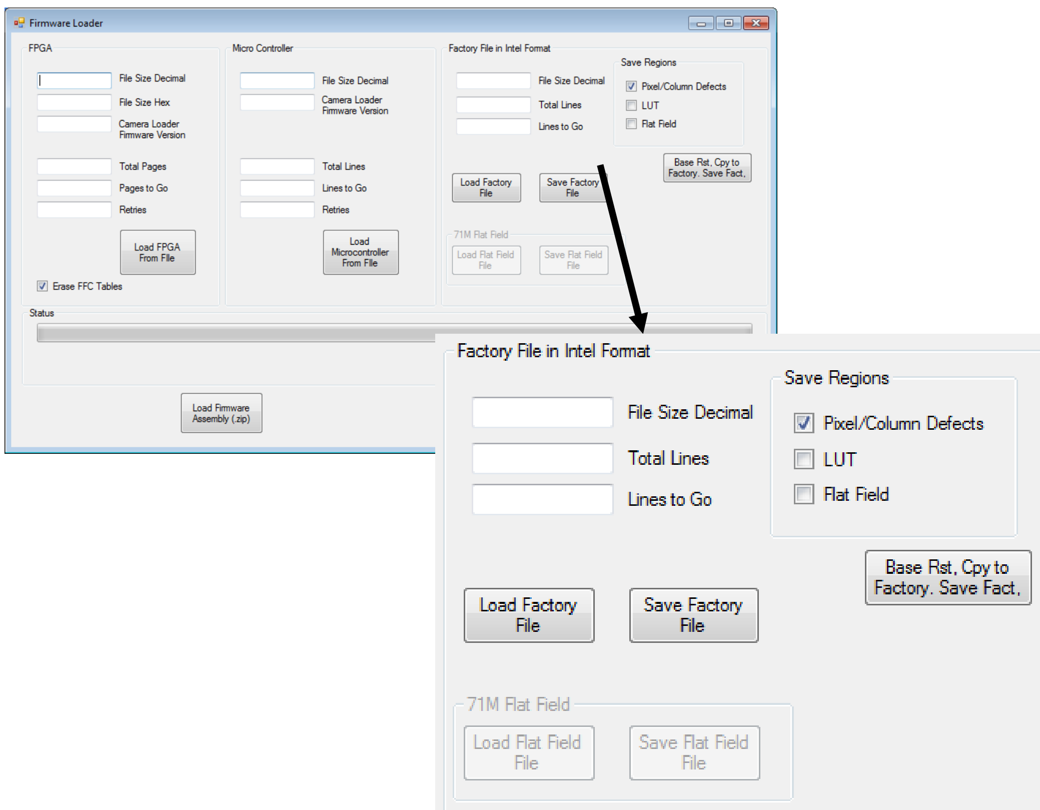
Backup/Restore

The COE-71 camera control program provides features for saving and restoring the camera state. Please save the camera state before changing the default state of the camera.

State data can be saved and restored (from files) for the following:

1) Camera state with optional defect tables.
2) Flat Field Calibration data.

Note: The camera control program may change the communication rate during this operation.



Camera Save/Restore

Save Factory File: Saves the camera state to a file for future restores. Options include defect table.

Load Factory File: Restores camera state from a file. The camera state is saved in manufacturing and can be emailed to the user.

Save FFC File: Saves the camera Flat Field Correction (FFC) to a file for future restores.

Load FFC File: Restores camera FFC from a file.

Overview

The COE-71 sensor operates with a rolling electronic shutter and integrates an internal signal sequencer for image readout.

The internal modes do not natively support the use of a trigger pulse width exposure control.

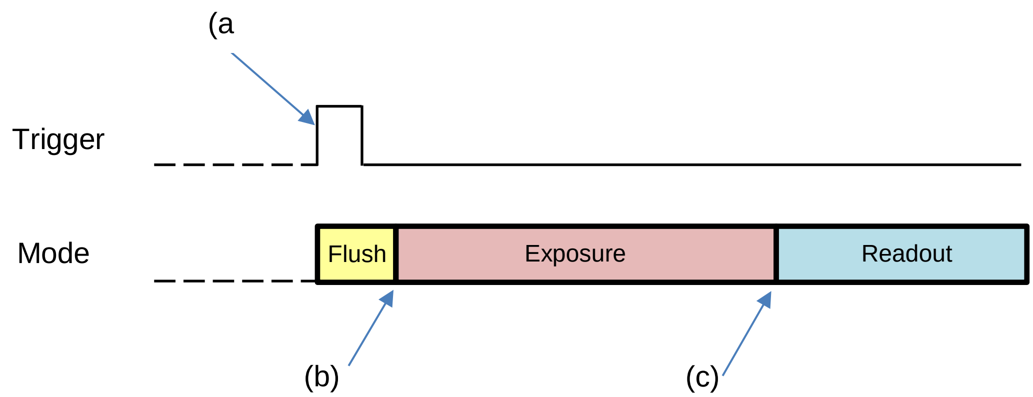
Opto Engineering has bypassed the limitations of the CHR70M sensor by designing a custom sensor sequencer that controls the sensor at a low level and provides new functionality as describe here:

A sensor flush mode : All lines of the sensor are erased in sequence. (< 1.5ms)

An externally controlled exposure: **Allows for exposure to be pulse width controlled**.

In addition, a programmable strobe output is provided for control of external synchronization to lighting. The following diagram shows the basic operation of the sequenced exposure:

(a) Trigger is asserted, flush begins.
(b) Each of the 7096 lines are reset, in order. Image exposure begins.
(c) Exposure of the sensor ends, readout begins.



Externally Sequenced Exposure

Pulse Width Exposure Control

The external sequencing of the CHR70M sensor allows for a true pulse width controlled exposure. In this mode, a trigger rising edge begins the exposure sequence and the trigger falling edge ends the exposure, and then begins the readout sequence.

Some details of the operation:

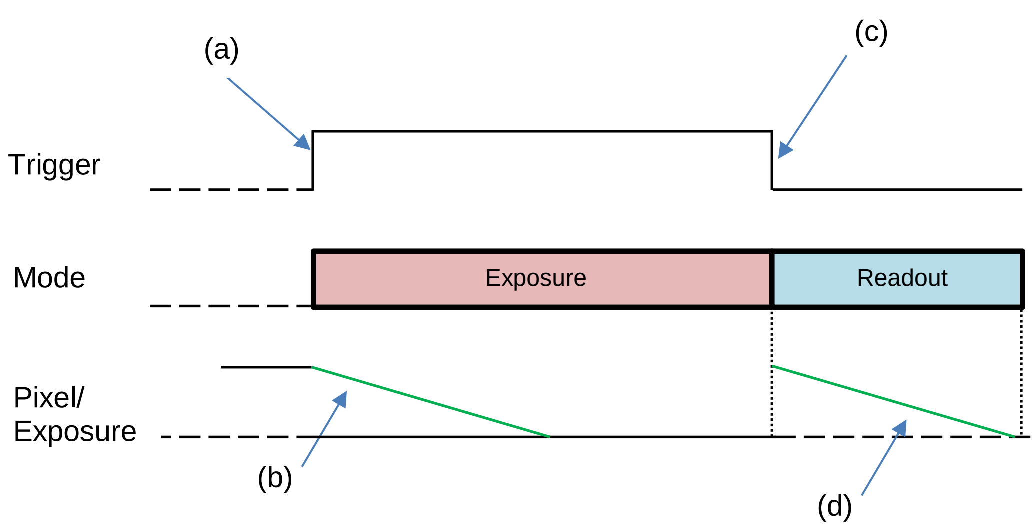
(a) Trigger is asserted, flush begins.

(b) Each of the 7096 lines are reset, in order. Image integration begins.

(c) Trigger is de-asserted, exposure of the sensor ends, readout begins.

(d) During readout pixels are integrating.

There are two flush modes, a standard line time flush mode, that will result in uniform exposed images, and a fast flush mode for specialized applications.



Externally Sequenced Pulse Width Exposure

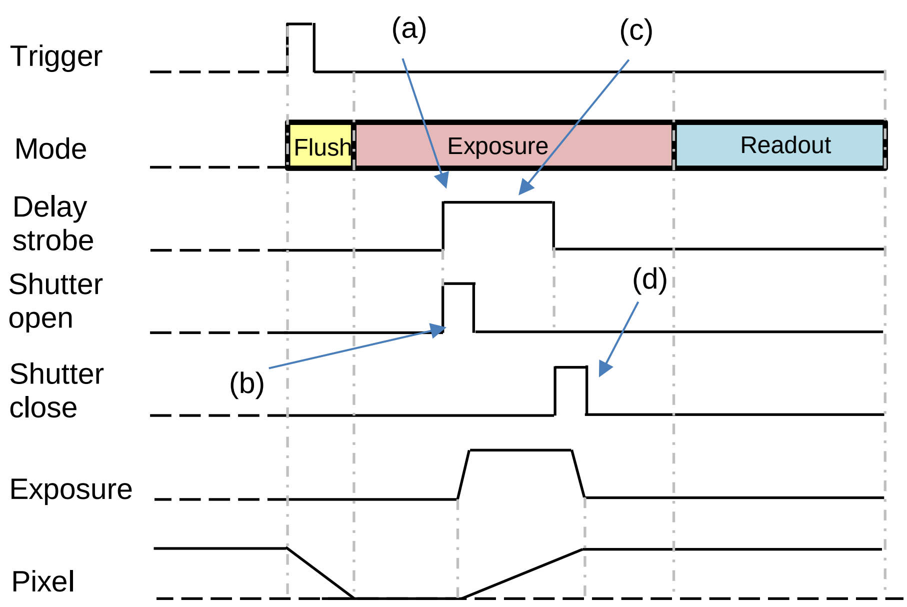
Triggered Mechanical Shutter

A mechanical shutter can be used in the external sequencing mode to provide a true global shutter operation of the CHR70M. In this mode the shutter controls the integration of the image. Flush, exposure and readout all work the same as before. The strobe output as well as the shutter open and close pulses are all programmable in delay and duration.

Some details of the operation:

(a) A programmable delay for both the strobe and shutter sequence is provided.
(b) The shutter open pulse is programmable in duration (usually set at the factory).
(c) A shutter/strobe delay is programmable.
(d) The shutter close pulse is programmable in duration (usually set at the factory). (Note: image integration ends at the close of the mechanical shutter).

This mode requires special hardware consisting of a mechanical shutter, lens mount and electronics. The fast flush mode is used in this application.



Mechanical Shutter Exposure Overview

Triggered Pulse Width Mode

Triggered Pulse Width Mechanical Shutter

When using the mechanical shutter in pulse width exposure mode the shutter timing is as follows.

Some details of the operation:

(a) On trigger assert a shutter open sequence is initiated.

A programmable delay for both the strobe and shutter sequence is provided.

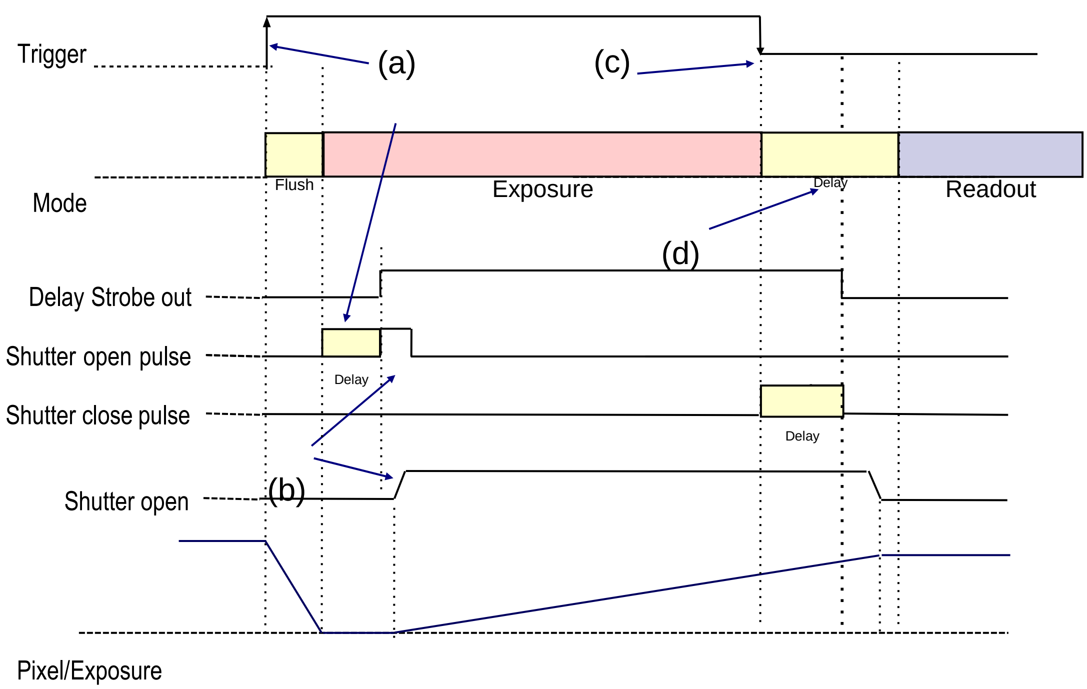
(b) The shutter open pulse is programmable in duration (usually set at the factory).

Depending on the shutter mechanics, the timing of the shutter open is delayed.

(c) On trigger de-assert a shutter close sequence is initiated.

(d) A delay from trigger de-assert to readout is provided to allow the mechanical shutter to close completely.

This mode requires special hardware consisting of a mechanical shutter, lens mount and electronics. The fast flush mode is used in this application.



Triggered Pulse Width Mechanical Shutter Exposure Overview

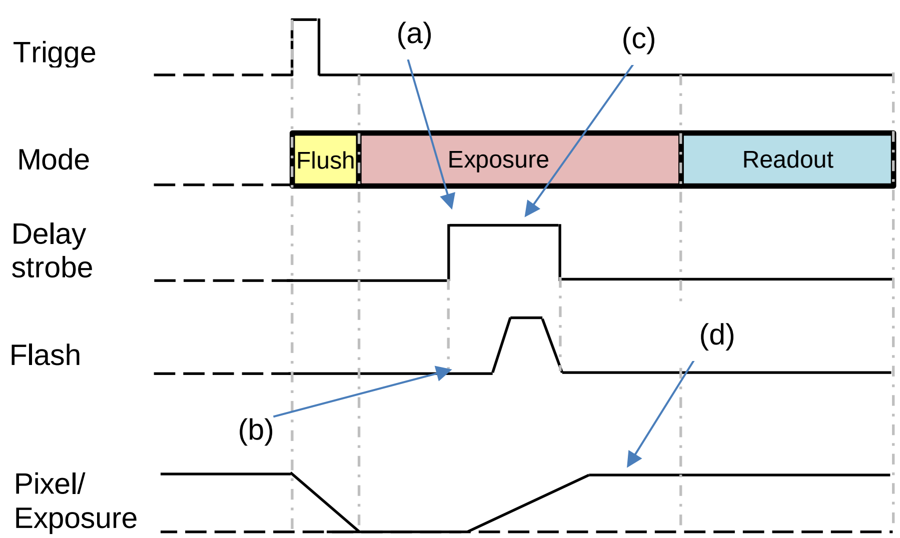
Triggered Flash Exposure

A Flash exposure can be used in the external sequencing mode to provide a true global shutter operation of the CHR70M. In this mode the flash controls the integration of the image. Flush, exposure and readout all work the same as before. The sensor must operate and readout in complete darkness for the flash operation to function correctly.

Some details of the operation:

(a) A programmable delay for the strobe is provided to sync the flash.
(b) The flash illumination determines the exposure.
(c) The strobe duration is programmable.
(d) The readout of the image is in the dark so integration is constant.
(Note: image integration ends at the end of the flash).

This mode requires special hardware consisting of a external flash control and flash hardware. The fast flush mode is used in this application.



Triggered Flash Exposure Overview

Triggered Flash Exposure Continued

The flash timing is as follows:

(a) Assert trigger

(b) Camera performs fast flush of sensor, flash is delayed until flush complete.

The flush time for each readout mode is:

Base mode 21.25Mhz: 2.34ms

Medium mode 30Mhz : 1.65ms

Medium mode 42.5Mhz : 1.17ms

(c) Exposure begins

(d) Flash is asserted from camera strobe output

(e) Programmed exposure ends and image is readout

The time for each readout mode is:

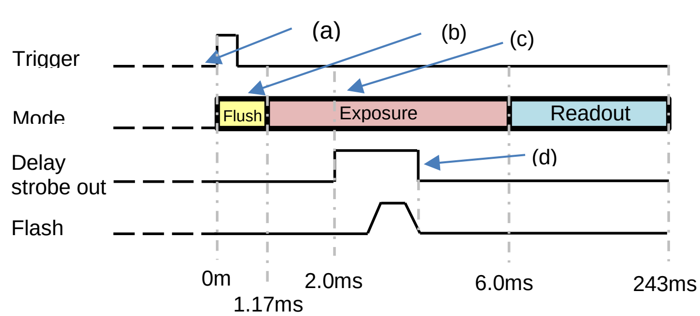
Base mode 21.25Mhz: 474ms

Medium mode 30Mhz : 333ms

Medium mode 42.5Mhz : 237ms

Example:

Set the readout mode to medium 40Mhz	{w04000002fe}
Set the sequenced exposure mode active	{w02430001ff}
Set the programmed exposure mode active	{w04030001ff}
Set the exposure to 15,000 us (15ms)	{w02033A982e}
Set the fast flush mode	{w02220001ff}
Set the ms tick register to 42500	{w0216a60456}
Set the strobe delay to 2ms	{w02110002fe}
Set the strobe pulse width to 2ms	{w02120002fe}
Set the strobe delay enable	{w02100001ff}
Begin operation	
Or use Triggered Sequenced Flash	{w04030012ee}

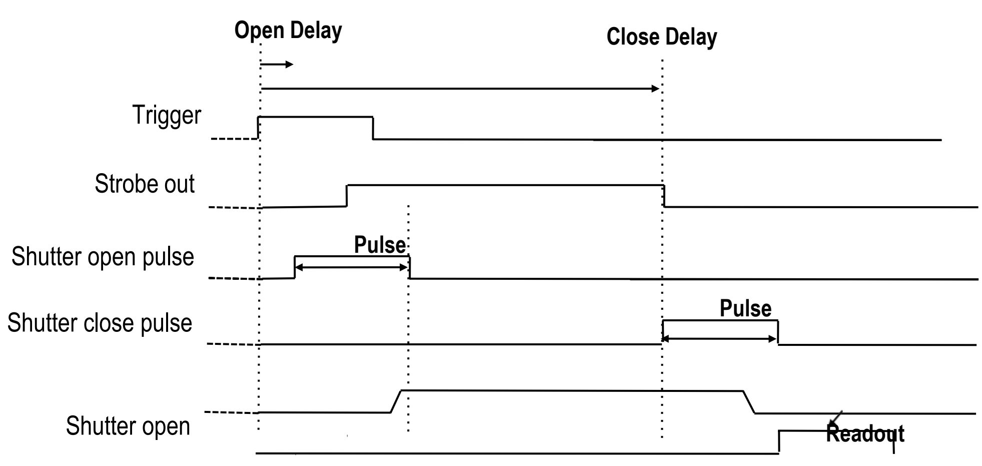


Triggered Pulse Width Shutter Exposure Details

Sequencer Mode Commands

These functions set the parameters associated with the external triggered modes and shutter/flash strobe output.

Target	Index	Description	Read Write	Modes
0x02	0x43	0=disable, 1=enable	R/W	Set External Programmed Exposure
0x04	0x03	1=enable	R/W	Set External Programmed Mode
0x04	0x03	2=enable	R/W	Set External Pulse Width Mode
0x02	0x10	0=normal, 1=delay	R/W	Set Strobe output mode
0x02	0x11	Data = ms delay	R/W	Set Strobe Delay
0x02	0x12	Data = ms dura-tion	R/W	Set Strobe Duration
0x02	0x14	Data = ms dura-tion	R/W	Set Shutter Duration (Pulse Width)
0x02	0x17	Data = ms delay	R/W	Set Shutter Open Delay
0x02	0x18	Data = ms delay	R/W	Set Shutter Close Delay
0x02	0x19	Data = ms delay	R/W	Readout delay to allow the shutter to close.
0x02	0x20	0=disable, 1=enable	R/W	Triger echo on strobe out line.
0x02	0X21	0=normal, 1=Manual	R/W	Manual Strobe Control
0x02	0x22	0=normal, 1=fast	R/W	Fast flush during Trig Pulse Width Mode
0x04	0x03	0x0012	W	**Sequenced Triggered Flash** Exposure = 15ms Strobe delay = 2/3/3ms (base, med30,med40) Strobe width = 10ms



Shutter

RO Delay

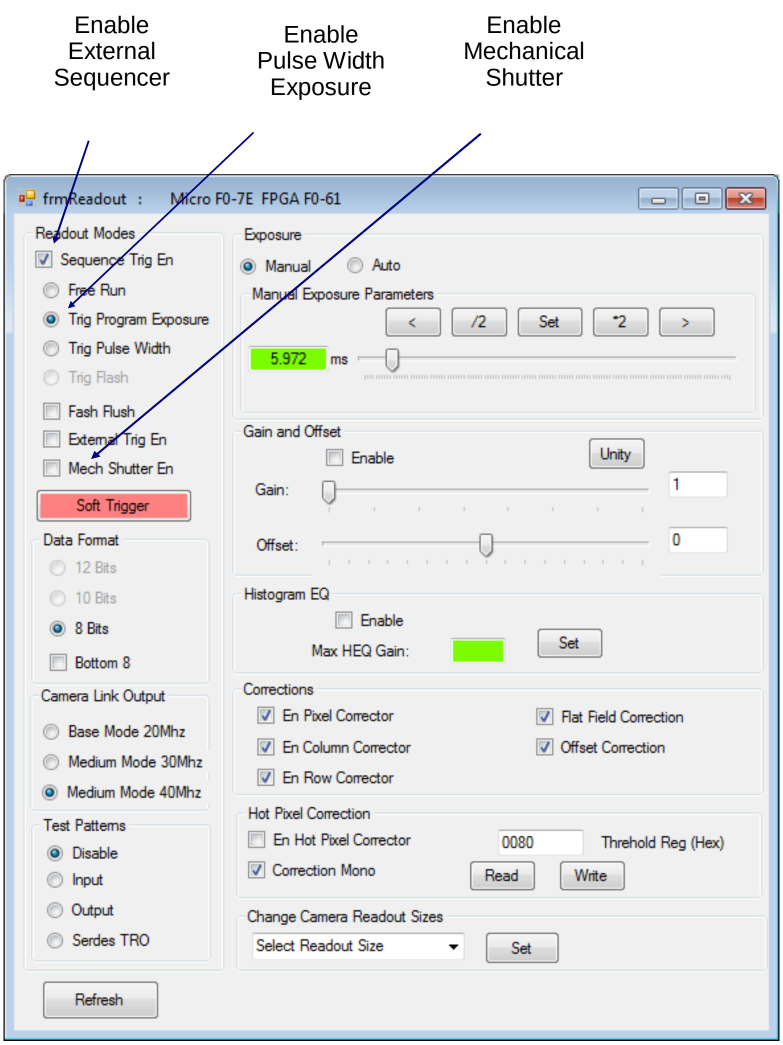
Readout Sensor

Camera Control Application Support

The Opto Engineering control application has been extended to provide control of these new features. The most important feature is the selection between internal and external sequencing modes (Sequence Trig En). In the external mode, pulse width exposure control is enabled.

Strobe and shutter controls are also provided for flash and mechanical shutter modes.

The exposure and readout dialog is shown below.



Triggered Pulse Width Mode

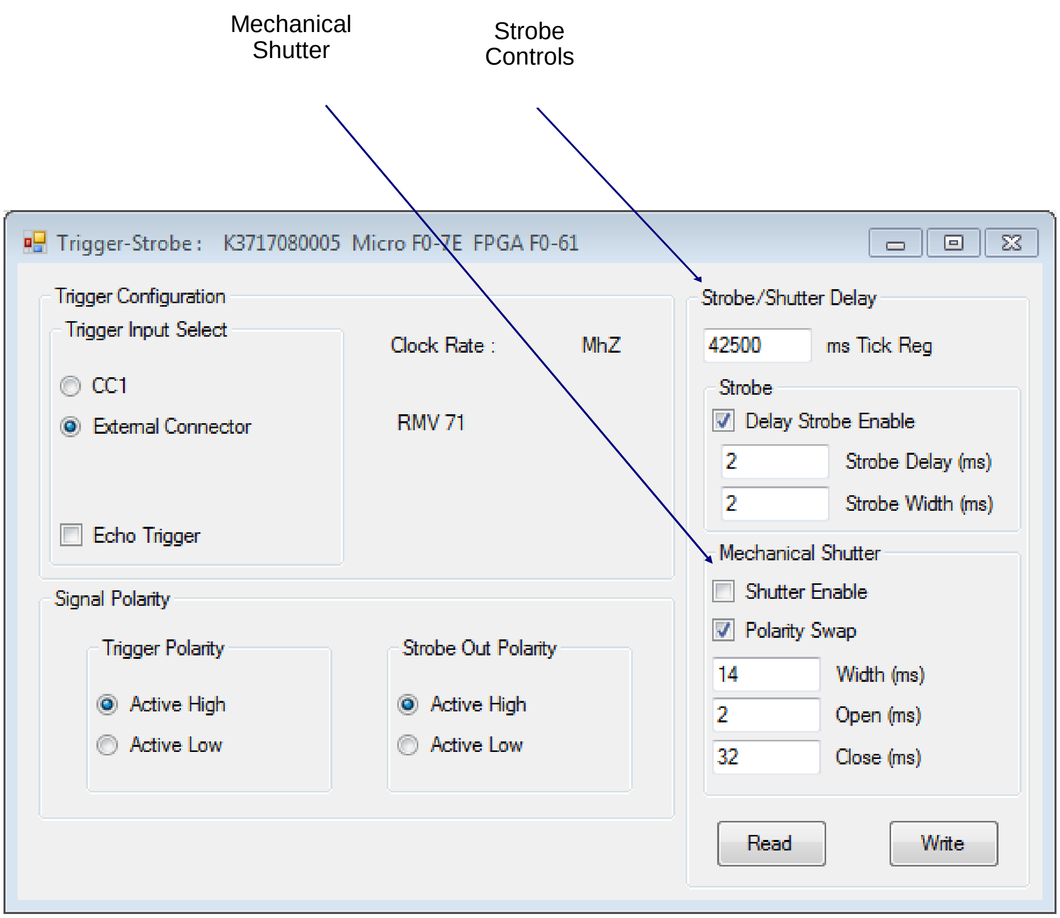
Strobe and mechanical shutter operation is controlled from the 'Trigger Strobe' dialog. The 'ms Tick register' controls the timing of the pulses by dividing the pixel clock to generate a ms clock. For each mode set it to the following:

Base mode 21.25Mhz:	21250
Medium mode 30Mhz :	33333
Medium mode 42.5Mhz :	42500

Note that the strobe can be set to echo the incoming trigger for debugging purposes.

Other debug modes are provided (Signal output on strobe signal)

Strobe debug off :	{wFE0f000000}
Flush (fast) timing :	{wFE0F00B749}
Expose (fast) timing :	{wFE0F00c739}
Readout (fast) timing :	{wFE0F00D729}



Firmware Update

COE-71 firmware is updated using the Opto Engineering control application by following these steps:

(1) Update to the recommended control application.

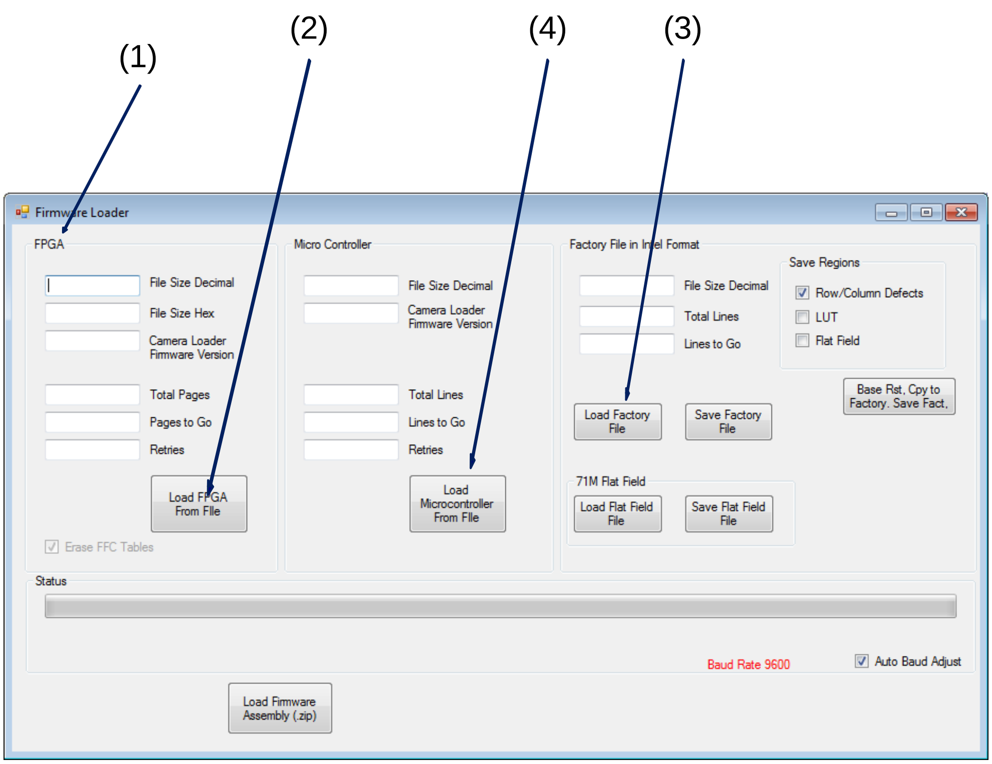
(2) Update the FPGA file with the ***.bin** file and the firmware loader dialog

(3) Update the EEPROM configuration with the ***.fca** file

(4) Update the microprocessor with the ***.hex** file

(5) Repower the camera, reopen the control app, reconfigure the camera settings.

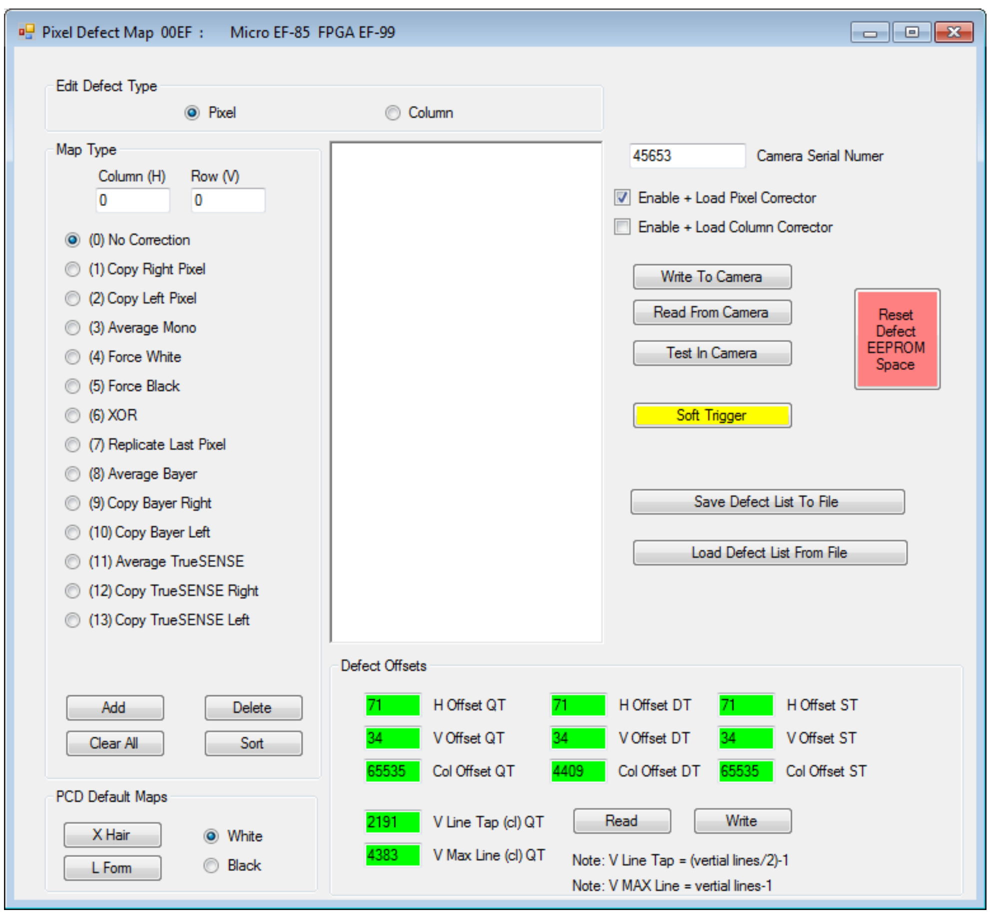
(6) If needed recalibrate the black offset and bright FFC.



Pixel, Column and Row Defects

Defect correction is used to “map out “ defective pixels in the camera and substitute synthesized pixel values. The Opto Engineering Camera Control Application provides a defect editor to simplify the editing of defect mapping.

Target	Index	Description	Read Write	Modes
0x04	0x1c	Defect Correction (DC)	Write	0x0000 = Load/Enable Pixel DC 0x0001 = Load/Enable Column DC 0x000A = Load/Enable Row DC 0x0005 = Disable Pixel DC 0x0004 = Disable Column DC 0x000B = Disable Row DC



Black Offset and Flat Field Correction

The CHR71M sensor used in the COE-71 camera requires image processing for optimal operation. The sensor incorporates a dark field Offset Correction on the chip. The Offset Correction will correct the 16 column analog offsets through digital to analog converters. The sensor also requires a Digital Gain for each of the 10,000 columns. The Column Gain corrects non-uniformity of the sensor analog paths. The following image shows the effects of Offset and Gain Correction.

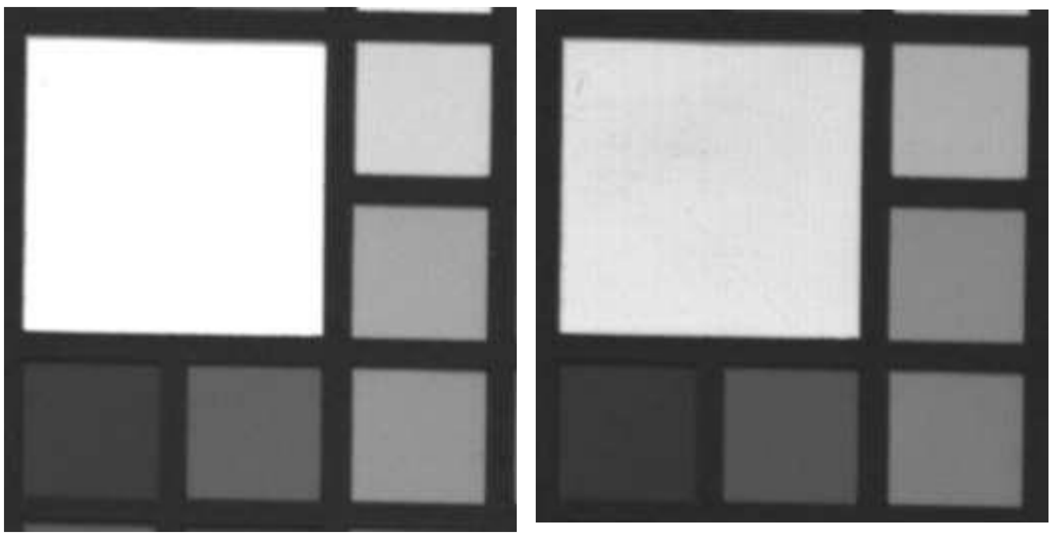


Image with (left) and without (right) Column Gain Correction

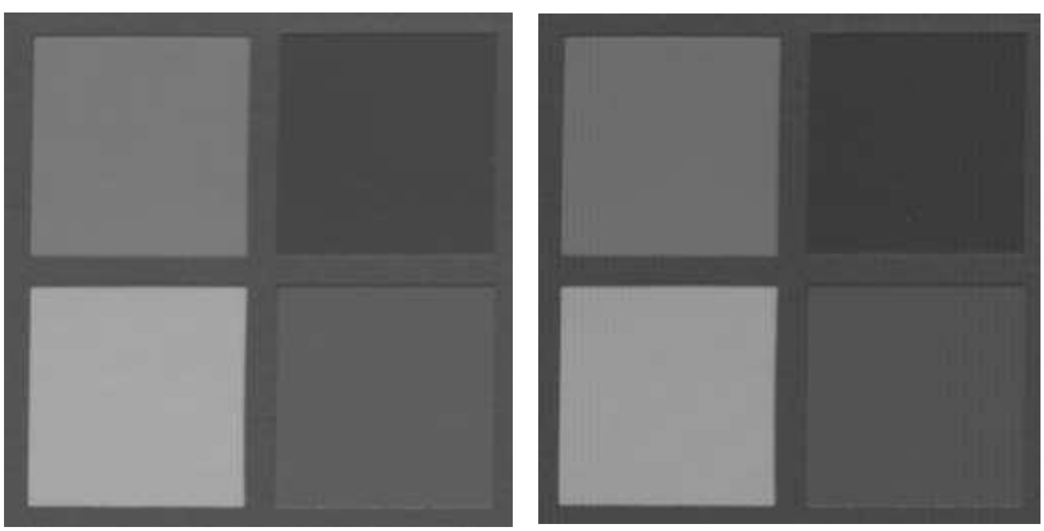


Image with (left) and without (right) 16 Column Offset Correction

Flat Field Correction

Warning: Changing the Flat Field Correction (FFC) tables will impact the operation of the camera. Before resetting the FFC, make sure the current FFC table is saved to a file. Files can be saved and reloaded using the Camera Control Application.

The image processing features of the COE-71 camera can be easily setup by using the following procedure:

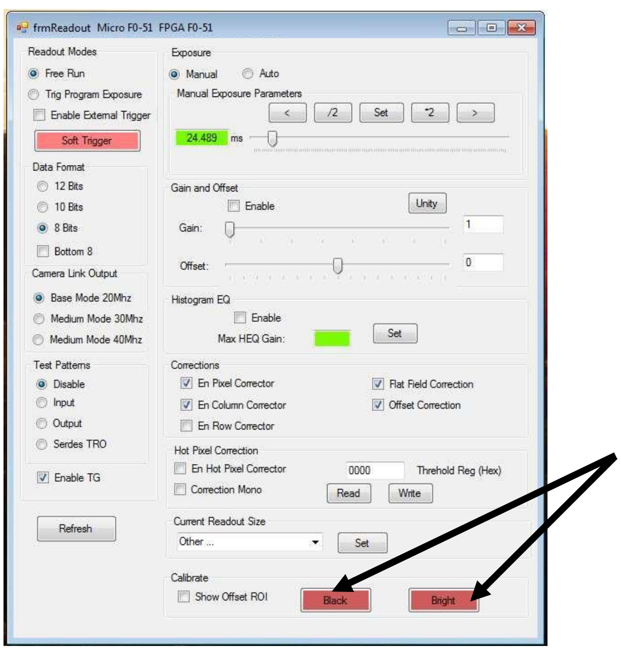
For 16 Column Offset Correction: Use the lens cap or light blocking device. This test is performed in the dark; therefore, no special equipment is needed. Only 16 words of data are stored for this correction.

For Column Gain Correction: Use the flat field light source. This can be as simple as a white balance lens cap and a flat background or "s" complex as a programmable light source. The flatter the field presented to the sensor the better the correction will be. The COE-71 processes the flat field in two passes, one for the even numbered columns and one for the odd numbered columns. A total of 10,000 Column Gains are calculated and saved in the EEPROM of the camera. This process may take over a minute to complete.

For optimum performance, the Offset and Gain calculations should be calculated under the conditions that the camera is used and should include the following parameters:

- Operating temperature.
- Exposure.
- Readout mode and pixel clock speed.

It is recommended to perform the Black (offset) calibration first followed by the Bright (gain) calibration.



Exposure and Readout Dialog

The exposure and readout dialog contains the controls for calibrating the Offset (dark) and Column Gain (bright). The Column Gain (FF) can be enabled along with the defect corrections for pixel, row, and columns.

Note: ***Extend the dialog box by dragging the bottom to see the controls***

Column Gain Correction (Bright)

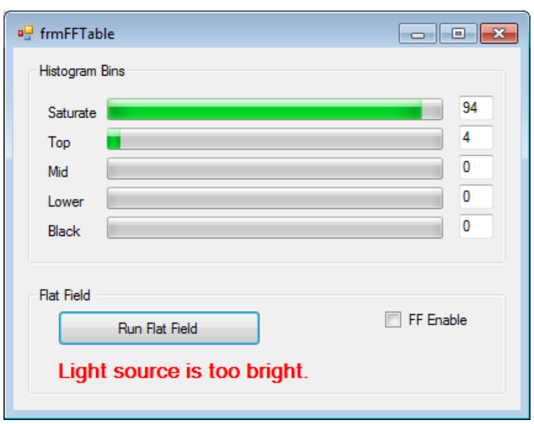
The Bright (column gain) calibration will present a dialog box with the 5 point histogram. The top two bar graphs represent the saturated pixels as well as the top 10% pixel counts. These two values must be zero to continue with the calibration.

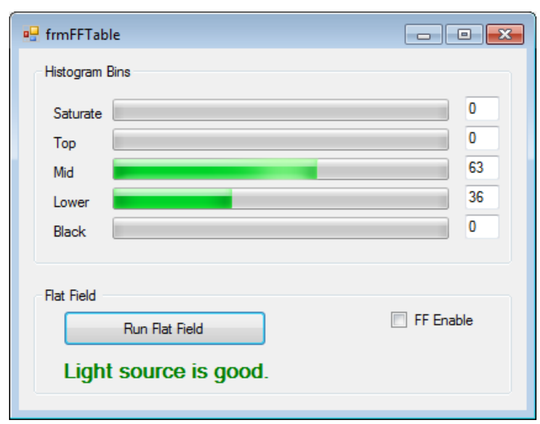
Note: The image must be uniform (flat) to obtain correct calibration.

- Adjust the intensity of the light source so that the adjustment dialog reports the light source as “good”.
- Press the “Run Flat Field” button. The calibration will complete and the Column Gains will be activated in the camera (but not saved to EEPROM).
- Examine the calibration result. If acceptable, press the “Save To EEPROM” button to save the results.

Note: Currently only one calibration can be saved to EEPROM.

Note: Saving to EEPROM can take several minutes. Watch the On Screen Display (OSD) frame count as it will restart once the save is complete. DO NOT POWER DOWN THE CAMERA DURING EEPROM WRITE.





Offset Calibration

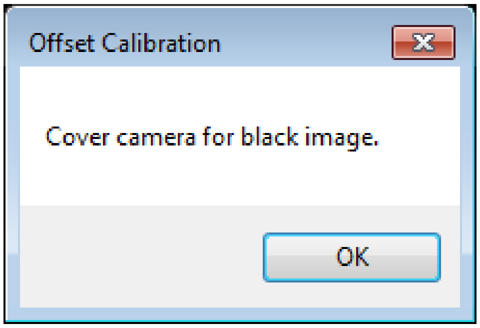
Offset Correction (Black)

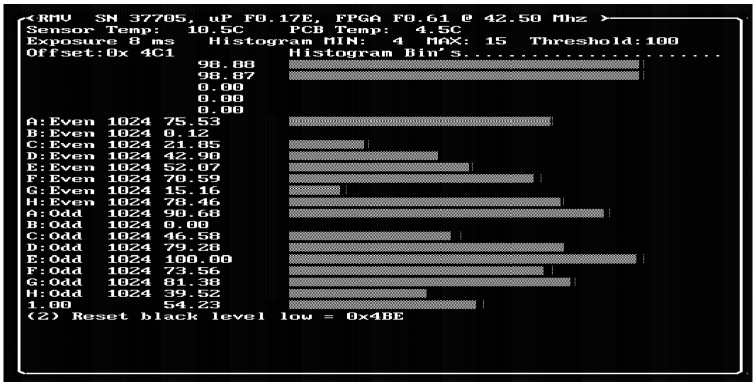
The Black (offset) calibration will present a dialog box asking the lens to be covered in order to obtain a completely dark image.

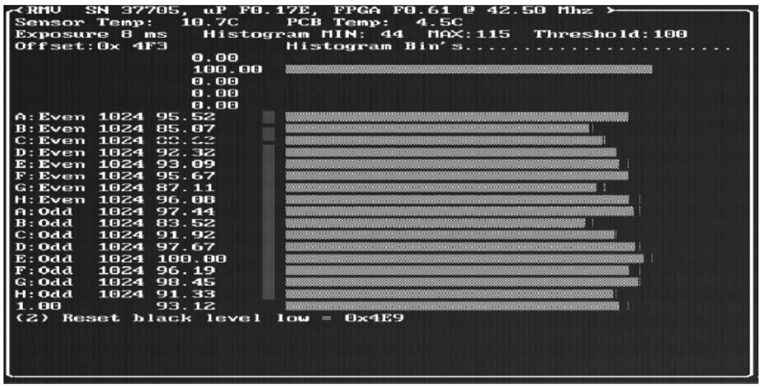
Clicking OK will start the Offset Calibration and an on-screen display will be activated to show the progress.

A series of bar graphs will display the current offset values and relative brightness. As the calibration proceeds the values will converge. Once an acceptable solution is found, the calibration data will be saved to EEPROM and the results will display in the OSD.

The lens cap may now be removed and the camera used.







Histogram Equalization

Histogram Equalization

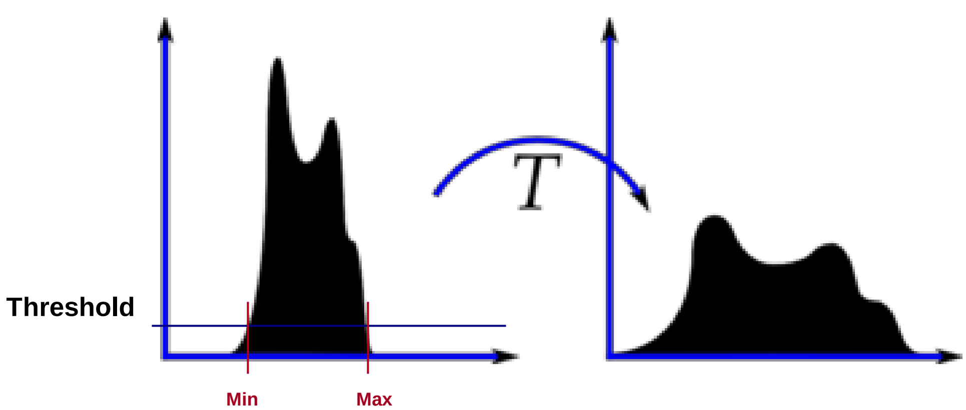
The Histogram Equalization (HEQ) function is provided for applications that need to dynamically adjust the incoming image data to a full output range. This is typically needed in surveillance applications where image data is viewed but not measured.

The Histogram Detector calculates a 512 point histogram, based on the image data within the brightness (AED) detector. The histogram is then measured using a threshold to determine its minimum and maximum values.

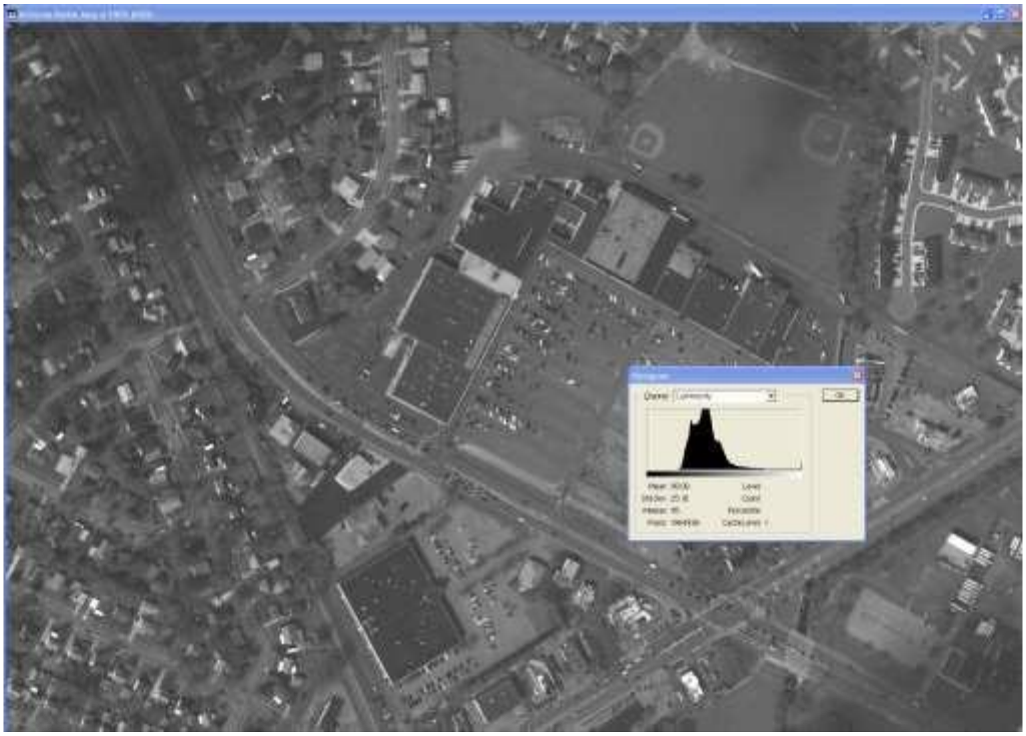
The minimum value is used to set the Master Digital Offset register, which shifts the histogram to restore the black level. The maximum value is used to calculate the gain needed to equalize the histogram to full range. This value is set in the Master Digital Gain register.

The Equalized Histogram is fit to 90% of the range to compensate for data lost by thresholding. The histogram endpoints are not considered in the equalization so that saturated pixels do not skew the equalization.

Target	Index	Description	Read Write	Modes
0x04	0x60	Histogram EQ Enable	R/W	0 = disable
0x04	0x61	Histogram Threshold	R/W	Range 0x00..0xFF,
0x04	0x62	Histogram Detector Enable	R/W	0 = disable
0x04	0x63	Maximum HEQ Gain	R/W	Max digital gain in HEQ mode
0x04	0x24	Digital Gain	R/W	
0x04	0x30	Digital Offset	R/W	
0x04	0x38	Master DGO Enable	R/W	1 = enable, 0 = disable



Histogram Equalization



Low contrast image before Histogram Equalization

Low contrast image after Histogram Equalization

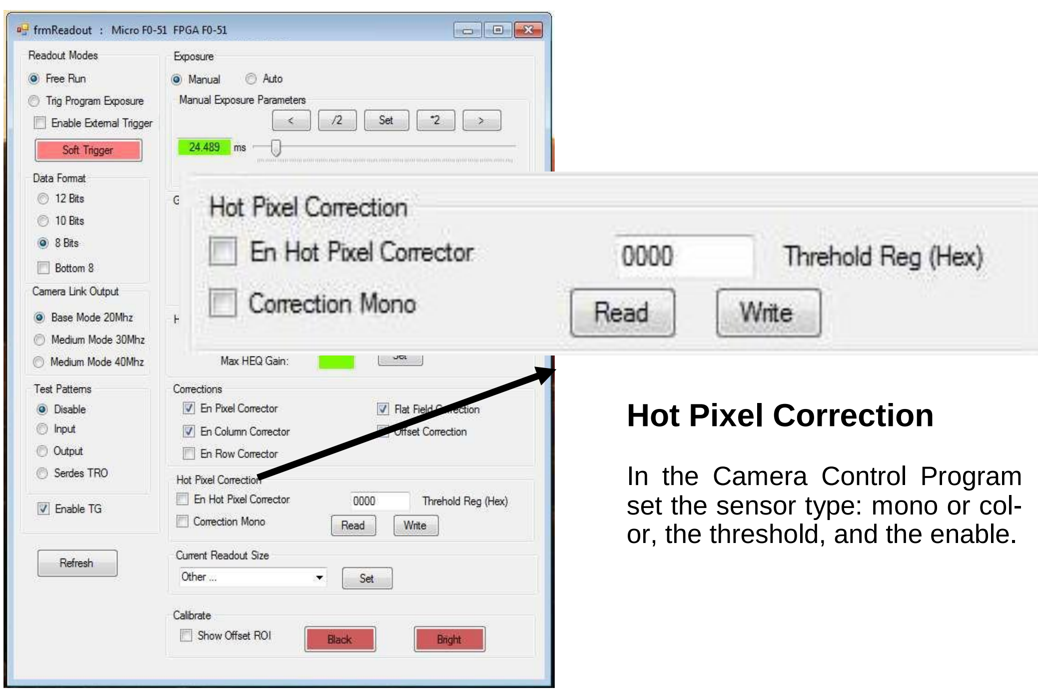
Hot Pixel Correction

The Hot Pixel Correction (HPC) algorithm dynamically analyzes the video data for single bright (hot) pixels.

Hot pixels are generated by thermal noise in the photo diode of the sensor. Long exposures will create more hot pixels than short exposures.

The HPC does not require calibration. It compares a target pixel with its horizontally adjacent pixels. The difference of left/right neighbor and the pixel is calculated. If the difference is greater than the set **Threshold,** then the pixel is replaced with the average of the adjacent pixels.

Target	Index	Description	Read Write	Modes
0x04	0xA0	Hot Pixel Corrector	R/W	0x0000 = Disabled 0x0001 = Enabled
0x04	0xA1	Hot Pixel Correction Type	R/W	0x0000 = Color Bayer 0x0001 = Monochrome
0x04	0xA2	Hot Pixel Threshold	R/W	Threshold in dn Recommended > 0x0010



Hot Pixel Correction

In the Camera Control Program set the sensor type: mono or color, the threshold, and the enable.

Hot Pixel Correction

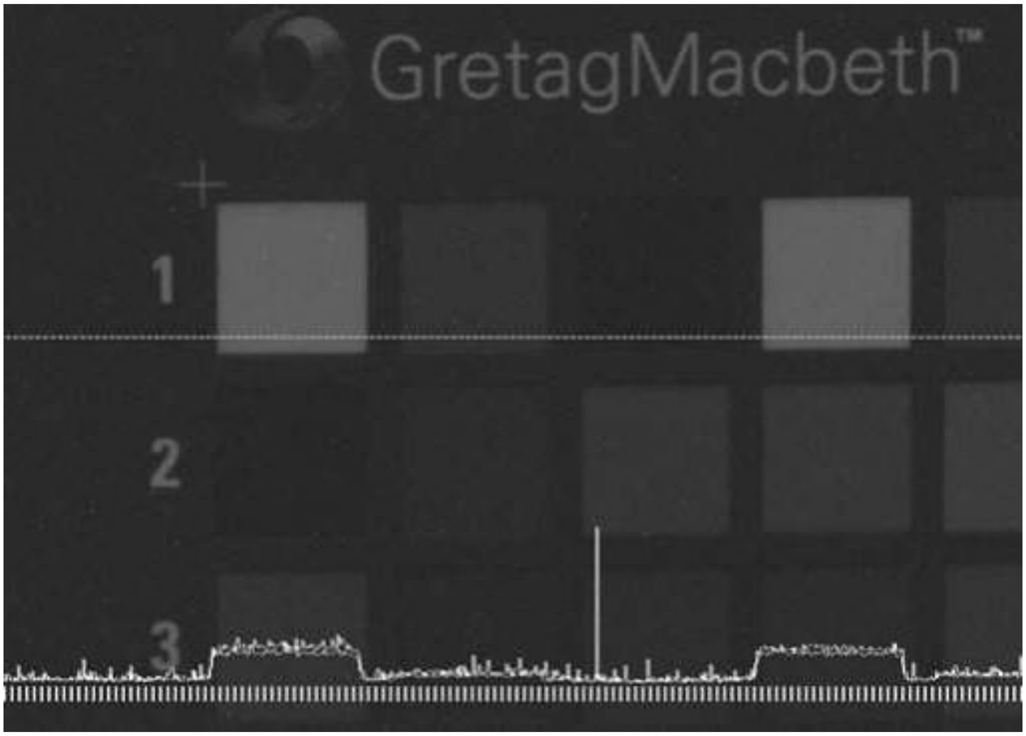


Image with Hot pixels

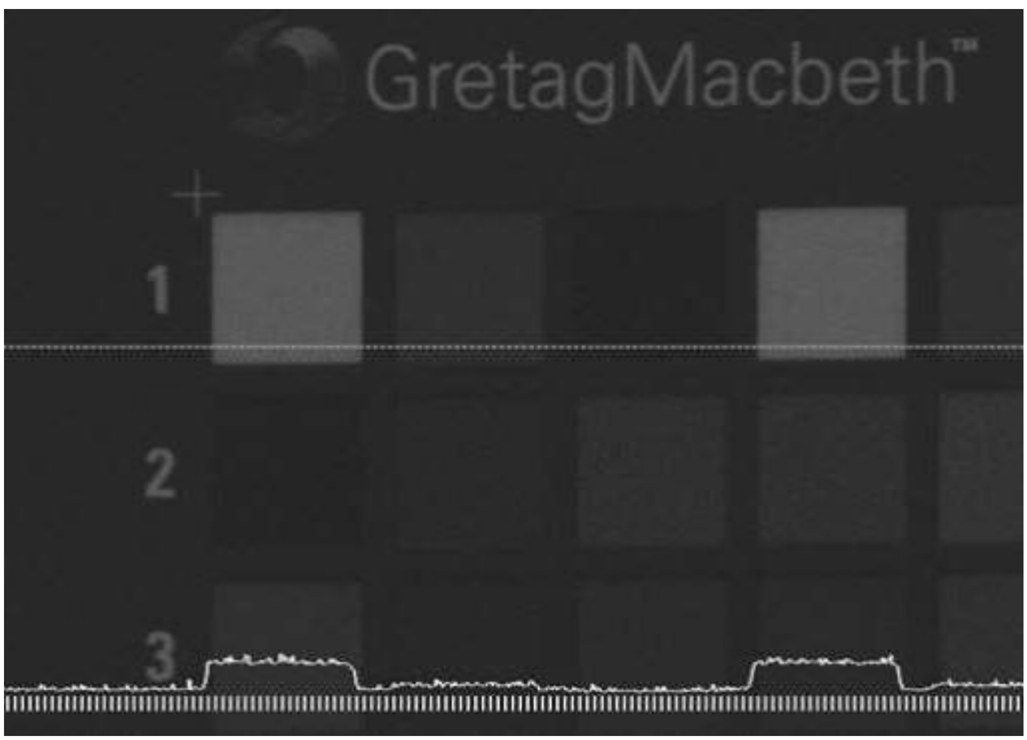


Image with Corrected Hot pixels

Long Exposures

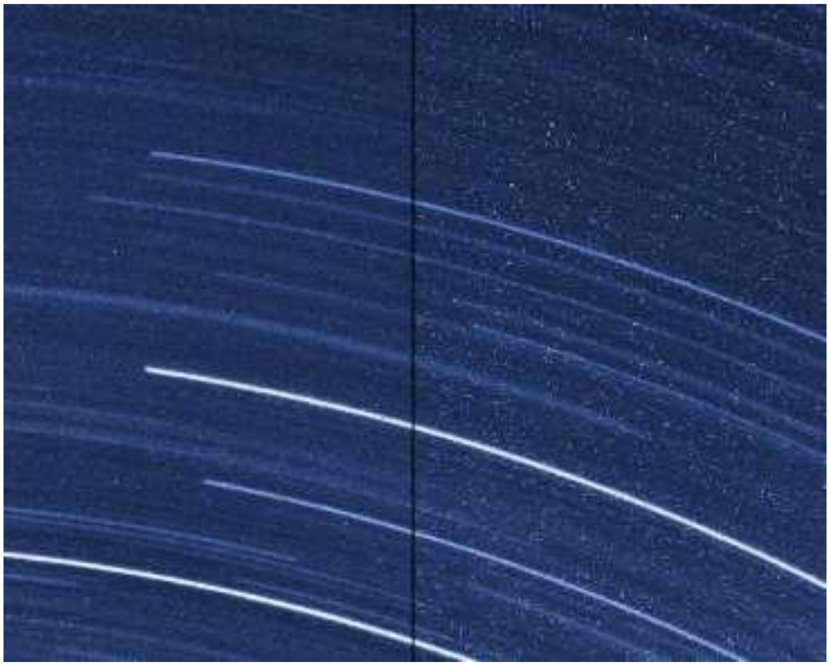
The CMV-71 uses the ams/CMOSIS CHR71M sensor. This sensor is implemented in a CMOS process with 3.1µm pixels, and as such does not perform as well as CCD sensors with larger pixels. In particular the dark current performance is approximately 4.5x worse than a typical Interline CCD sensor with 5.5µm pixels.

These are the recommended techniques to minimize the dark current:

1) Reduce the camera and sensor operating temperature.
2) Utilize a dark frame subtraction algorithm.
3) Break longer exposures into many short exposures, subtract a dark frame and sum the images.
4) Use the Hot Pixel Corrector feature.

The CHR71M specifications (v6) for Dark Signal:

Dark Noise	7e -	(measured in high gain mode)
Dark Signal	3.2 e-/s	at Room Temperature
DSNU	6 e/s	at Room Temperature
Full Well	> 13ke	



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